Section 25. Device Configuration

HIGHLIGHTS

This section of the manual contains the following major topics:

25.1 INTRODUCTION

The device Configuration registers allow each user to customize certain aspects of the device to fit the needs of the application. Device Configuration registers are nonvolatile locations in program memory that hold settings for the dsPIC® DSC device during power-down. The Configuration registers hold global setup information for the device, such as the oscillator source, Watchdog Timer (WDT) mode, code protection settings and others.

The device Configuration registers are mapped in program memory locations, starting at address 0xF80000, and are accessible during normal device operation. This region is also referred to as 'configuration space'.

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations.

25.2 DEVICE CONFIGURATION REGISTERS

Each device Configuration register is a 24-bit register. However, only the lower 16 bits of each register hold configuration data. Nine device Configuration registers are available to user software:

- **FBS: Boot Code Segment Configuration Register**
- **FSS: Secure Code Segment Configuration Register**
- **FGS: General Code Segment Configuration Register**
- **FOSCSEL: Oscillator Source Selection Register**
- **FOSC: Oscillator Configuration Register**
- **FWDT: Watchdog Timer (WDT) Configuration Register**
- **FPOR: POR Configuration Register**
- **FICD: In-Circuit Debugger Configuration Register**
- **FCMP: Comparator Configuration Register**

The device Configuration registers can be programmed using Run-Time Self-Programming (RTSP), In-Circuit Serial Programming™ (ICSP™) or a device programmer.

Note:	Some Configuration registers and bits may not be present on all dsPIC33F devices. Refer to the specific device data sheet for more information.

Register 25-1: FBS: Boot Code Segment Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	U-0	U-0	R/P	R/P	R/P	R/P
RBS<1:0>		—	—	BSS<2:0>			BWRP
bit 7							bit 0

nb

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7-6 **RBS<1:0>:** Boot Segment RAM Code Protection bits
11 = No Boot RAM defined
10 = Boot RAM is 128 bytes
01 = Boot RAM is 256 bytes
00 = Boot RAM is 1024 bytes

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3-1 **BSS<2:0>:** Boot Segment Program Flash Code Protection Size bits
Refer to the specific device data sheet for more information.

bit 0 **BWRP:** Boot Segment Program Flash Write Protection bit
1 = Boot segment can be written
0 = Boot segment is write-protected

Register 25-2: FSS: Secure Code Segment Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	U-0	U-0	R/P	R/P	R/P	R/P
RSS<1:0>		—	—	SSS<2:0>			SWRP
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7-6 **RSS<1:0>:** Secure Segment RAM Code Protection bits
11 = No Secure RAM defined
10 = Secure RAM is 256 bytes, less BS RAM
01 = Secure RAM is 2048 bytes, less BS RAM
00 = Secure RAM is 4096 bytes, less BS RAM

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3-1 **SSS<2:0>:** Secure Segment Program Flash Code Protection Size bits
Refer to the specific device data sheet for more information.

bit 0 **SWRP:** Secure Segment Program Flash Write Protection bit
1 = Secure segment can be written
0 = Secure segment is write-protected

Register 25-3: FGS: General Code Segment Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
—	—	—	—	—	GSS<1:0>		GWRP
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-3 **Unimplemented:** Read as ‘0’

bit 2-1 **GSS<1:0>:** General Segment Code-Protect bits
11 = User program memory is not code-protected
10 = Standard security
0x = High security

bit 0 **GWRP:** General Segment Program Flash Write Protection bit
1 = General segment may be written
0 = General segment is write-protected

Register 25-4: FOSCSEL: Oscillator Source Selection Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	U-0	U-0	U-0	U-0	R/P	R/P	R/P
IESO	—	—	—	—	FNOSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7 **IESO:** Two-Speed Start-up Enable bit
1 = Start device with FRC, then automatically switch to the user-selected oscillator source when ready
0 = Start device with the user-selected oscillator source

bit 6-3 **Unimplemented:** Read as ‘0’

bit 2-0 **FNOSC<2:0>:** Initial Oscillator Source Selection (IOSC) bits
111 = Internal Fast RC (FRC) oscillator with postscaler
110 = Internal FRC oscillator with divide-by-16
101 = LPRC oscillator
100 = Secondary (LP) oscillator
011 = Primary (XT, HS, EC) oscillator with PLL
010 = Primary (XT, HS, EC) oscillator
001 = Internal FRC oscillator with PLL
000 = FRC oscillator

Register 25-5: FOSC: Oscillator Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	R/P	U-0	U-0	R/P	R/P	R/P
FCKSM<1:0>		IOL1WAY	—	—	OSCIOFNC	POSCMD<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7-6 **FCKSM<1:0>:** Clock Switching Mode bits
1x = Clock switching is disabled; Fail-Safe Clock Monitor (FSCM) is disabled
01 = Clock switching is enabled; FSCM is disabled
00 = Clock switching is enabled; FSCM is enabled

bit 5 **IOL1WAY:** Peripheral Pin Select (PPS) Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 4-3 **Unimplemented:** Read as ‘0’

bit 2 **OSCIOFNC:** OSC2 Pin Function bit (except in XT and HS modes)
1 = OSC2 is clock output
0 = OSC2 is general purpose digital I/O pin

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode Select bits
11 = Primary Oscillator disabled
10 = HS Crystal Oscillator mode
01 = XT Crystal Oscillator mode
00 = EC (External Clock) mode

Register 25-6: FWDT: Watchdog Timer (WDT) Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	R/P	U-0	U-0	R/P	R/P	R/P
FWDTEN	WINDIS	PLLKEN	WDTPRE	WDTPOST<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7 **FWDTEN:** Watchdog Timer (WDT) Enable Mode bit
1 = WDT always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect)
0 = WDT enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)

bit 6 **WINDIS:** Watchdog Timer (WDT) Window Enable bit
1 = WDT in Non-Window mode
0 = WDT in Window mode

bit 5 **PLLKEN:** Phase-Locked Loop (PLL) Enable bit
1 = Clock switch to the PLL source will wait until the PLL lock signal is valid
0 = Clock switch will not wait for PLL lock

bit 4 **WDTPRE:** Watchdog Timer (WDT) Prescaler bit
1 = 1:128
0 = 1:32

bit 3-0 **WDTPOST<3:0>:** Watchdog Timer (WDT) Postscaler bits
1111 = 1:32,768
1110 = 1:15,384
•
•
•
•
0001 = 1:2
0000 = 1:1

Register 25-7: FPOR: POR Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
PWMPIN	HPOL/ALTQIO	LPOL/ALTSS1	ALTI2C	BOREN	FPWRT<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as '0'

bit 7 **PWMPIN:** Motor Control PWM Module Pin Mode bit
1 = PWM module pins controlled by PORT register at device Reset (tri-stated)
0 = PWM module pins controlled by PWM module at device Reset (configured as output pins)

bit 6 **HPOL:** Motor Control PWM High-Side Polarity bit
1 = PWM module high-side output pins have active-high output polarity
0 = PWM module high-side output pins have active-low output polarity

ALTQIO: Alternate QEI1 Pins bit
1 = QEI1 mapped to QEA1A, QEB1A, and INDX1A pins
0 = QEI1 mapped to QEA1, QEB1, and INDX1 pins

bit 5 **LPOL:** Motor Control PWM Low-Side Polarity bit
1 = PWM module low-side output pins have active-high output polarity
0 = PWM module low-side output pins have active-low output polarity

ALTSS1: Alternate $\overline{SS1}$ Pin bit
1 = SPI1 mapped to $\overline{SS1A}$ pin
0 = SPI1 mapped to $\overline{SS1}$ pin

bit 4 **ALTI2C:** Alternate I^2C™ Pins bit
1 = I^2C mapped to SDA1/SCL1 pins
0 = I^2C mapped to ASDA1/ASCL1 pins

bit 3 **BOREN:** Brown-out Reset (BOR) Enable bit
1 = BOR is enabled
0 = BOR is disabled

bit 2-0 **FPWRT<2:0>:** Power-on Reset (POR) Timer Value Select bits
111 = PWRT = 128 ms
110 = PWRT = 64 ms
101 = PWRT = 32 ms
100 = PWRT = 16 ms
011 = PWRT = 8 ms
010 = PWRT = 4 ms
001 = PWRT = 2 ms
000 = PWRT = Disabled

Note: Refer to the specific device data sheet for more details on bit descriptions.

Register 25-8: FICD: In-Circuit Debugger Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

r	r	R/P	U-0	U-0	U-0	R/P	R/P
—	—	JTAGEN	—	—	—	ICS<1:0>	
bit 7							bit 0

Legend:			
r = Reserved	R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7-6 **Reserved:** Do not use

bit 5 **JTAGEN:** JTAG Enable bit
1 = JTAG is enabled
0 = JTAG is disabled

bit 4-2 **Unimplemented:** Read as ‘0’

bit 1-0 **ICS<1:0>:** ICD Communication Channel Select Enable bits
11 = Communicate on PEGC1 and PGED1
10 = Communicate on PEGC2 and PGED2
01 = Communicate on PEGC3 and PGED3
00 = Reserved, do not use

Register 25-9: FCMP: Comparator Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/P	R/P	R/P	R/P	R/P	R/P
—	—	CMPPOL1	HYST1<1:0>		CMPPOL0	HYST0<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-6 **Unimplemented:** Read as '0'

bit 5 **CMPPOL1:** Comparator Hysteresis Polarity bit (for odd numbered comparators)
1 = Hysteresis is applied to falling edge
0 = Hysteresis is applied to rising edge

bit 4-3 **HYST1<1:0>:** Comparator Hysteresis Select bits
11 = 45 mV hysteresis
10 = 30 mV hysteresis
01 = 15 mV hysteresis
00 = No hysteresis

bit 2 **CMPPOL0:** Comparator Hysteresis Polarity bit (for even numbered comparators)
1 = Hysteresis is applied to falling edge
0 = Hysteresis is applied to rising edge

bit 1-0 **HYST0<1:0>:** Comparator Hysteresis Select bits
11 = 45 mV hysteresis
10 = 30 mV hysteresis
01 = 15 mV hysteresis
00 = No hysteresis

25.3 CONFIGURATION BIT DESCRIPTIONS

This section provides functional information for each of the device Configuration bits.

25.3.1 Code Protection and CodeGuard™ Security

The dsPIC33F product families offer advanced security, which protects the intellectual property that users invest in collaborative system designs. CodeGuard™ Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip with assurance that their intellectual property rights are not at risk.

The Code Protection features are controlled by the Configuration registers (FBS, FSS and FGS) and vary from one dsPIC33F device to another. For more details, refer to the specific device data sheet, and refer to **Section 23. "CodeGuard™ Security"** (DS70199).

25.3.2 Oscillator Configuration Bits

The dsPIC33F clock selection, switching, and configuration settings are controlled by the Oscillator Source Selection (FOSCSEL) and Oscillator Configuration (FOSC) registers, and the PLLKEN bit in the Watchdog Timer Configuration (FWDT) register. For more details, refer to **Section 7. "Oscillator"** (DS70186).

25.3.3 POR Configuration Bits

The POR Configuration bits, found in the FPOR Configuration register, are used to set the Power-up Timer delay time. For more details on these Configuration bits, refer to **Section 8. "Reset"** (DS70192).

25.3.4 Motor Control PWM Module Configuration Bits

The Motor Control PWM module Configuration bits are located in the FPOR Configuration register and are present only on devices that have the PWM module. The Configuration bits associated with the PWM module perform the following two functions:

- Select the state of the PWM pins at a device Reset (high Z or output).
- Select the active signal polarity for the PWM pins. The polarity for the high-side and low-side PWM pins can be selected independently.

For more details on these Configuration bits, refer to **Section 14. "Motor Control PWM"** (DS70187).

25.3.5 Watchdog Timer (WDT) Configuration Bits

The dsPIC33F WDT can be enabled and configured using the Watchdog Timer Configuration Register (FWDT). For more details on these Configuration bits, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196).

25.3.6 JTAG Interface

The dsPIC33F device family implements a JTAG interface, which supports boundary scan device testing, as well as in-circuit programming. Detailed information on this interface is provided in future revisions of the document.

Note:	Refer to **Section 24. "Programming and Diagnostics"** (DS70207), for more details on usage, configuration and operation of the JTAG interface.

25.3.7 In-Circuit Serial Programming™ (ICSP™)

The ICSP™ capability is Microchip's proprietary process for microcontroller programming in the target application. The ICSP interface uses two pins as its core. The programming data pin (PGEDx) functions as both an input and an output, allowing programming data to be read in and device information to be read out on command. The programming clock pin (PGECx) clocks in data and controls the overall process.

Serial programming allows customers to manufacture boards with unprogrammed devices and then to program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. For more details on ICSP, refer to the "*dsPIC33F/PIC24H Flash Programming Specification*" (DS70152).

Any of the following three pairs of programming clock/data pins can be used:

- PGEC1/PGED1
- PGEC2/PGED2
- PGEC3/PGED3

During programming, each pin pair is recognized as a valid programming connection. Therefore, no special selection is to be performed by the user to specify which pin pair will be used for programming.

25.3.8 In-Circuit Debugger

When the MPLAB® ICD 3 or MPLAB REAL ICE™ in-circuit emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging when used with MPLAB IDE. The debugging functionality is controlled through the PGECx (emulation/debug clock) and PGEDx (emulation/debug data) pin functions.

Any of the following three pairs of debugging clock/data pins can be used:

- PGEC1/PGED1
- PGEC2/PGED2
- PGEC3/PGED3

The debugging clock and data pins must be selected by programming the ICD Communication Channel Select Enable (ICS<1:0>) bits in the In-Circuit Debugger Configuration (FICD<1:0>) register. To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS}, and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

25.4 DEVICE IDENTIFICATION REGISTERS

The dsPIC33F devices have two set of registers located in configuration space that provide identification information.

25.4.1 Device ID (DEVID) Registers

Configuration memory space locations 0xFF0000 and 0xFF0002 are used to store a read-only Device ID number that is set when the device is manufactured. This number identifies the dsPIC33F device type and the silicon revision. The Device ID registers can be read using table read instructions.

25.4.2 Unit ID Field

The Unit ID field is located at configuration memory space locations 0xF80010 through 0xF80016. This field consists of four Configuration registers (FUID0-FUID3) and can be programmed with unique device information.

25.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Device Configuration include the following:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F family of devices.

25.6 REVISION HISTORY

Revision A (February 2007)

This is the initial release of this section.

Revision B (February 2007)

Minor edits throughout document.

Revision C (January 2008)

This revision includes the following corrections and updates:

- Sections:
  - Added **25.3.6 “JTAG Interface”**
  - Added **25.3.7 “In-Circuit Serial Programming™ (ICSP™)”**
  - Added **25.3.8 “In-Circuit Debugger”**
- Registers:
  - Updated FOSCSEL: Oscillator Source Selection register (see Register 25-4)
  - Updated FPOR: POR Configuration register (see Register 25-7)
  - Added FICD: In-Circuit Debugger Configuration register (see Register 25-8)
- Tables:
  - Updated register map table (see Table 25-1)

Revision D (January 2009)

This revision includes the following corrections and updates:

- Registers:
  - Added the PLLKEN bit to the Watchdog Timer Configuration (FWDT) register (see Register 25-6).
  - Removed the BKBUG and COE bits from the In-Circuit Debugger Configuration (FICD) register (see Register 25-8).
- Updated **25.3.2 “Oscillator Configuration Bits”** to include a reference to the PLLKEN bit
- Additional minor corrections such as language and formatting updates have been incorporated throughout the document.

Revision E (August 2009)

This revision includes the following corrections and updates:

- Note:
  - Added a note in Register 25-7.
- Registers:
  - Updated unimplemented bits to read as ‘0’ in all the registers:
    U = Unimplemented bit, read as '1' is updated as U = Unimplemented bit, read as '0'.
  - Added new bit name and bit descriptions for bit 5 and bit 6 in Register 25-7.
  - Updated the bit name as “r” for bit 6 and bit 7 in Register 25-8.
  - Updated the Legend “r = Reserved” in Register 25-8.
  - Added the **FCMP: Comparator Configuration Register** (see Register 25-9).
- Sections:
  - Updated the **25.3.7 “In-Circuit Serial Programming™ (ICSP™)”** section for selection of programming pins.
  - Changed all instances of PGCx/EMUCx and PGDx/EMUDx (where x = 1, 2, or 3) to PGECx and PGEDx
  - Removed the Register Map section (Section 25.5).
- Additional minor corrections such as language and format updates have been incorporated throughout the document.