Section 24. Device Configuration

HIGHLIGHTS

This section of the manual contains the following topics:

24.1 Introduction

The device Configuration registers allow each user to customize certain aspects of the device to fit the needs of the application. Device Configuration registers are nonvolatile memory locations in the program memory map that hold settings for the dsPIC device during power-down. The Configuration registers hold global setup information for the device, such as the oscillator source, Watchdog Timer mode and code protection settings.

The device Configuration registers are mapped in program memory locations, starting at address 0xF80000 and are accessible during normal device operation. This region is also referred to as “configuration space”.

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’) to select various device configurations.

24.2 Device Configuration Registers

Each device Configuration register is a 24-bit register, but only the lower 16 bits of each register are used to hold configuration data. There are four device Configuration registers available to the user:

- FOSC (0xF80000): Oscillator Configuration Register **(Note 2)**
- FWDT (0xF80002): Watchdog Timer Configuration Register
- FBORPOR (0xF80004): BOR and POR Configuration Register
- FGS (0xF8000A): General Code Segment Configuration Register

The device Configuration registers can be programmed using Run-Time Self-Programming (RTSP), In-Circuit Serial Programming™ (ICSP™), or by a device programmer.

Note 1: Not all device Configuration bits shown in the subsequent Configuration register descriptions may be available on a specific device. Refer to the device data sheet for more information.

2: dsPIC30F devices in the General Purpose, Sensor and Motor Control families feature one of three versions of the Oscillator system – Version 1, Version 2 and Version 3. For information on the Configuration bits of the FOSC device Configuration register available in each of these versions, please refer to **Section 7. "Oscillator"**.

Register 24-1: FWDT: Watchdog Timer Configuration Register

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
R/P	U	U	U	U	U	U	U
FWDTEN	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U	U	R/P	R/P	R/P	R/P	R/P	R/P
		FWPSA<1:0>		FWPSB<3:0>			
bit 7							bit 0

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **FWDTEN:** Watchdog Enable Configuration bit
1 = Watchdog Enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register. Will have no effect.)
0 = Watchdog Disabled (LPRC oscillator can be disabled by clearing the SWDTEN bit in the RCON register.)

bit 14-6 **Unimplemented:** Read as '0'

bit 5-4: **FWPSA<1:0>:** Prescale Value Selection for Watchdog Timer Prescaler A bits
11 = 1:512
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-0 **FWPSB<3:0>:** Prescale Value Selection for Watchdog Timer Prescaler B bits
1111 = 1:16
1110 = 1:15
•
•
•
0001 = 1:2
0000 = 1:1

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 24-2: FBORPOR: BOR and POR Configuration Register

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
R/P	U	U	U	U	R/P	R/P	R/P
MCLREN	—	—	—	—	PWMPIN	HPOL	LPOL
bit 15							bit 8

Lower Byte:							
R/P	U	R/P	R/P	U	U	R/P	R/P
BOREN	—	BORV<1:0>		—	—	FPWRT<1:0>	
bit 7							bit 0

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **MCLREN:** $\overline{\text{MCLR}}$ Pin Function Enable bit
1 = Pin function is $\overline{\text{MCLR}}$ (default case)
0 = Pin is disabled

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **PWMPIN:** Motor Control PWM Module Pin Mode bit
1 = PWM module pins controlled by PORT register at device Reset (tri-stated)
0 = PWM module pins controlled by PWM module at device Reset (configured as output pins)

bit 9 **HPOL:** Motor Control PWM Module High Side Polarity bit
1 = PWM module high-side output pins have active-high output polarity
0 = PWM module high-side output pins have active-low output polarity

bit 8 **LPOL:** Motor Control PWM Module Low Side Polarity bit
1 = PWM module low-side output pins have active-high output polarity
0 = PWM module low-side output pins have active-low output polarity

bit 7 **BOREN:** PBOR Enable bit
1 = PBOR Enabled
0 = PBOR Disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **BORV<1:0>:** Brown-out Voltage Select bits
11 = 2.0V
10 = 2.7V
01 = 4.2V
00 = 4.5V

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **FPWRT<1:0>:** Power-on Reset Timer Value Selection bits
11 = PWRT = 64 ms
10 = PWRT = 16 ms
01 = PWRT = 4 ms
00 = Power-up timer disabled

Note: PWMPIN, HPOL, and LPOL Configuration bits are only available on devices that feature a Motor Control PWM module.

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 24-3: FGS: General Code Segment Configuration Register

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U	U	U	U	U	U	P	P
—	—	—	—	—	—	GCP	GWRP
bit 7							bit 0

bit 23-2 **Unimplemented:** Read as '0'

bit 1 **GCP:** General Code Segment Code-Protect bit
1 = User program memory is not code-protected
0 = User program memory is code-protected

bit 0 **GWRP:** General Code Segment Write-Protect bit
1 = User program memory is not write-protected
0 = User program memory is write-protected

Note: The BCP and GWRP Configuration bits can only be programmed to a '0'.

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

24.3 Configuration Bit Descriptions

This section provides specific functional information on each of the device Configuration bits.

24.3.1 Oscillator Configuration Bits

dsPIC30F devices in the General Purpose, Sensor and Motor Control families feature one of three versions of the Oscillator system – Version 1, Version 2 and Version 3. For information on the Configuration bits of the FOSC device Configuration register available in each of these versions, please refer to **Section 7. "Oscillator"**.

24.3.2 BOR and POR Configuration Bits

The BOR and POR Configuration bits found in the FBORPOR Configuration register are used to set the Brown-out Reset voltage for the device, enable the Brown-out Reset circuit, and set the Power-up Timer delay time. For more information on these Configuration bits, please refer to **Section 8. "Reset"**.

24.3.3 Motor Control PWM Module Configuration Bits

The motor control PWM module Configuration bits are located in the FBORPOR Configuration register and are present only on devices that have the PWM module. The Configuration bits associated with the PWM module have two functions:

1. Select the state of the PWM pins at a device Reset (high-Z or output).
2. Select the active signal polarity for the PWM pins. The polarity for the high side and low side PWM pins may be selected independently.

For more information on these Configuration bits, please refer to **Section 15. "Motor Control PWM"**.

24.3.4 General Code Segment Configuration Bits

The general code segment Configuration bits in the FGS Configuration register are used to code-protect or write-protect the user program memory space. The general code segment includes all user program memory with the exception of the interrupt vector table space (0x000000-0x0000FE).

If the general code segment is code-protected by programming the GCP Configuration bit (FGS<1>) to a '0', the device program memory cannot be read from the device using In-Circuit Serial Programming (ICSP), or the device programmer. Additionally, further code cannot be programmed into the device without first erasing the entire general code segment.

When the general segment is code-protected, user code can still access the program memory data via table read instructions, or Program Space Visibility (PSV) accesses from data space.

If the GWRP (FGS<0>) Configuration bit is programmed, all writes to the user program memory space are disabled.

24.3.4.1 General Code Segment Configuration Bit Group

The GCP and GWRP Configuration bits in the FGS Configuration register must be programmed/erased as a group. If one or both of the Configuration bits is programmed to a '0', a full chip erase must be performed to change the state of either bit.

Note:	If the code protection Configuration fuse group (FGS<GCP:GWRP>) bits have been programmed, an erase of the entire code-protected device is only possible at voltages, VDD >= 4.5 volts.

24.4 Device Identification Registers

The dsPIC30F devices have two sets of registers located in configuration space that provide identification information.

24.4.1 Device ID (DEVID) Registers

The configuration memory space locations 0xFF0000 and 0xFF0002 are used to store a read-only Device ID number that is set when the device is manufactured. This number identifies the dsPIC30F device type and the silicon revision.

The Device ID registers can be read by the user using table read instructions.

24.4.2 Unit ID Field

The Unit ID field is located at configuration memory space locations 0x800600 through 0x80063E. This field consists of 32 program memory locations and can be programmed at the Microchip factory with unique device information. This field cannot be written or erased by the user, but can be read using table read instructions.

Please contact Microchip technical support or your local Microchip representative for further details.

24.5 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Device Configuration module are:

Title	Application Note #
Using the dsPIC30F for Sensorless BLDC Control	AN901

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

24.6 Revision History

Revision A

This is the initial released revision of this document.

Revision B

This revision incorporates technical content changes for the dsPIC30F Device Configuration module.

Revision C

This revision incorporates all known errata at the time of this document update.

Revision D

Descriptions of three versions of the Oscillator Control module have been added. The definition of the FOSC Configuration register was moved to DS70054.