

Extending Relay Life by Switching at Zero Cross

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INTRODUCTION

This short technical brief describes how to implement a Zero-Cross Detect feature on the PIC16F1708 microcontroller. This will also be used to switch a 220V relay to a 220 volt AC motor. Switching the relay at the zero-crossing point reduces spark across the contacts, extending relay life, and also reduces EMI. Switching at the zero-crossing point reduces EMI in both relays and high-voltage solid-state switches.

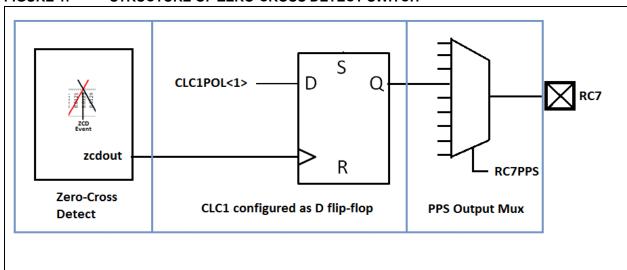
This application also demonstrates the "Core Independent Peripherals" concept, wherein interconnected peripherals are set up in advance of events, allowing fast switching with no processor interruption.

The zero-crossing detect event is routed through the CLC module to cause the switch to happen within microseconds of the zero-cross detect event occurring. Making use of the CLC for this function has numerous benefits:

- · Fast response to the zero-crossing event:
 - No CPU intervention required
 - Switching speed is independent of processor speed
 - Switch occurs on microsecond scale
- It frees CPU to handle other processes while events occur.
- It can operate while device is in Sleep to lower current consumption.

The zero cross has been structured such that the main program requests the switch, and the switch will occur at the next zero-cross rising edge event. The flip-flop receives its clock from the zero-cross detect output signal. The data into the flip-flop is controlled through the CLC1POL<1> bit. The data is routed to the RC7 output pin through the RC7PPS MUX.

FIGURE 1: STRUCTURE OF ZERO-CROSS DETECT SWITCH



This technical brief will provide the implementation for a motor switch. The user can switch the motor off and on with a momentary button press. The relay will be opened and closed at the zero-crossing point in order to extend the life of the relay contacts and reduce EMI. Switching at zero cross also has applications in power-factor correction.

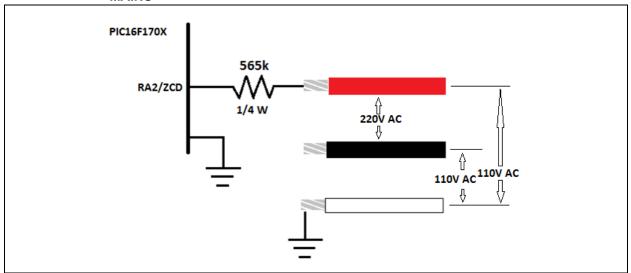
RESOURCE REQUIREMENTS

TABLE 1: RESOURCE REQUIREMENTS FOR ZERO-CROSS SWITCHING

CLC modules	1
RAM	1 byte
Program memory	119 of 4096 locations

PIC16F170X products are equipped with a zero-cross detect circuit. The zero-cross detect feature requires the use of one high-value resistor. It is important to use a large resistor to prevent overcurrent/overvoltage from damaging the PIC[®] device. The circuit diagram for zero-cross detect is shown below (Figure 2):

FIGURE 2: CONNECTION DIAGRAM FOR ZERO-CROSS PIN (RA2/ZCD) TO HIGH-VOLTAGE MAINS



Note that the zero-cross detect pin has been hooked to the red (hot) wire through the 565 k Ω resistor. It could optionally be hooked to the black (hot) wire. It is necessary that the ground be hooked to the white (common) wire.

The RA2/ZCD pin should nominally sink/source 300 μ A maximum. For a 120V (RMS) sine wave, it will have a peak of (120 *2^(1/2)) = 169.7V, using Ohm's law:

$$V/I = R = 169.7/300 \mu A = 565 k\Omega$$

The zero-cross detect peripheral has the option of generating interrupts on positive and negative-slope zero crossings. Two different power modes (High and Low) give flexibility in managing power consumption.

For this example, we are going to switch a 220V relay with a 12V DC coil. A push button switch (connected to pin RB7) is configured with an internal weak pull-up. The block diagram below (Figure 3) shows the primary connections:

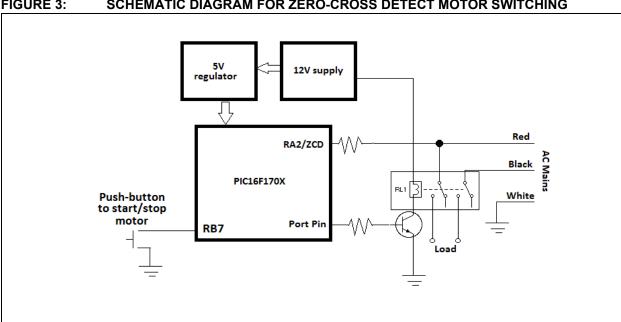
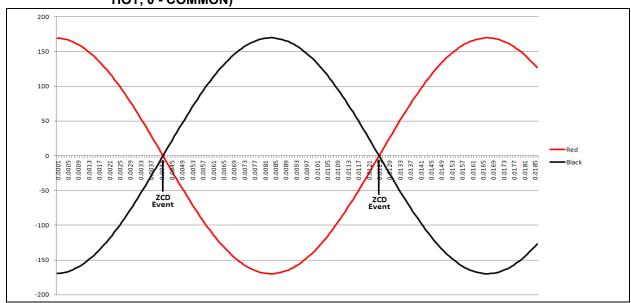


FIGURE 3: SCHEMATIC DIAGRAM FOR ZERO-CROSS DETECT MOTOR SWITCHING

AC VOLTAGE WAVEFORMS (60 Hz)

The voltages on the red and black power connections are sine waves which are 180° out of phase with each other. The graph below (Figure 4) shows AC waveforms and the zero-crossing point. Note that if we switch at the zero-crossing point for one of the "hot" wires, it will be the same as the zero-crossing for the other "hot" wire. 110V (RMS) is the voltage of red or black with respect to the center line. It is easy to see that by taking the potential between both wires (red and black) you have doubled the amplitude of voltage difference (220V RMS).

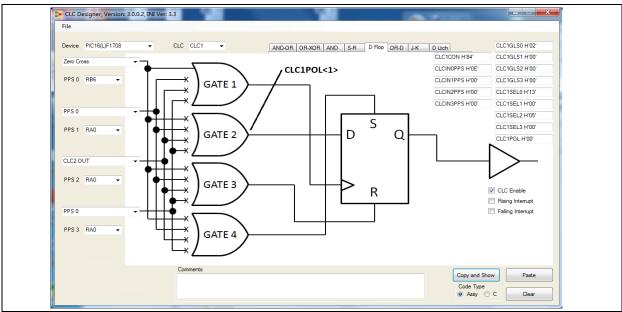
60 Hz AC MAIN WAVEFORMS AS A FUNCTION OF TIME (RED - HOT, BLACK -FIGURE 4: HOT, 0 - COMMON)



CLC CONFIGURATION

To switch near the zero-crossing point, we are feeding the clock of a D flip-flop with the zero-cross signal. The screen shot below (Figure 5) shows CLC1 configured as a D flip-flop with the clock fed from the zero-cross signal, and the data is provided via the CLC1POL<1> bit.

FIGURE 5: CLC DESIGNER TOOL WITH CLC1 CONFIGURED AS D FLIP-FLOP

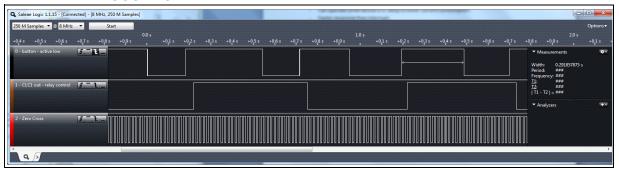


The logic waveform below (Figure 6) shows the following signals:

- Push button (active-low with internal pull-up from PIC device)
- · Relay switching signal
- Zero-cross detect signal (brought out on port pin through the CLC module).

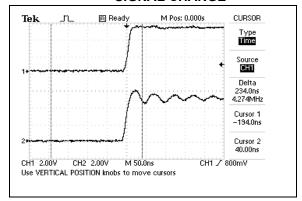
Notice that after each button press, there is a short delay to debounce the button, and then the state of the relay toggles. This allows a momentary push button to turn a motor on/off with successive presses. The change in CLC1OUT occurs on the rising edge of the zero-cross signal.

FIGURE 6: WAVEFORM SHOWING MULTIPLE BUTTON PRESSES AND RELAY OUTPUT TOGGLING



The next scope plot shows a zoomed-in view of the switch taking place at the zero-crossing point (Figure 7). The delay between the zero-cross signal and "CLC10UT" is solely gate propagation delay and is independent of the processor clock. The signals are almost simultaneous because the zero-cross signal is internal to the PIC device. Propagation delay in the CLC is negligible, but each signal sees the same delay at the respective output pad.

FIGURE 7: RELATIVE TIMINGS
BETWEEN ZERO-CROSS
RISING EDGE AND OUTPUT
SIGNAL CHANGE



CONCLUSION

It is our hope that this technical brief provides a starting point for developing applications using the zero-cross detect peripheral. Switching at zero cross reduces EMI. This may provide cost reductions for some applications by reducing PCB noise and filtering components.

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Code to switch the relay at the zero-crossing point is listed below.

```
#include "p16f1708.inc"
#define
            RELAY_CONTROL
                            CLC1POL,1
#define
                debounce_count 0x71
                                                  ; RAM location for debounce counter
start
    org 0x0000
         nop
                     ZCD1CON
         bsf
                      ZCD1CON, ZCD1EN
                                        ; Let's get started by turning on the Zero-cross detect module.
                     ANSELB
         banksel
         clrf
                  ANSELB
                                        ; make port B digital
                   0x04
         movwf
                   ANSELA
                                        ; make port A digital
                   0 \times 0.4
         movlw
                   ANSELC
         movwf
                                        ; make port C digital, except RC2.
                    TRISC
         banksel
         movlw
                    0x04
         movwf
                   TRISC
                                        ; port C all outputs, except RC2.
                   0xC0
         movlw
         movwf
                   TRISB
                                        ; port B all outputs, except RB7 and RB6
         movlw
                   0x04
         movwf
                   TRISA
                                        ; port A all outputs, except RA2.
         #include "zcd-clc1.inc"
                                     ; this sets up the CLC1 module as a d-type flip-flop
                                        ; with "zero-cross" as clock and data provided through CLC1POL<1>
         banksel
                     RC7PPS
                    0×04
         mowlw
         movwf
                   RC7PPS
                                         ; map CLC1 output (relay control) to RC7.
         banksel
                     RC6PPS
         movlw
                    0x13
         movwf
                   RC6PPS
                                         ; map "Zero-Cross" to RC6 (for visualization)
         banksel WPUA
          clrf
                   WPUA
                                      ; make sure weak pull-up is not turned on for RA2/ZCD
                     OPTION REG
         banksel
         bcf
                      OPTION REG, 7
                                      ; enable weak pull-ups.
main loop
         banksel
                     PORTR
         btfsc
                   PORTB, 7
                                         ; Is button depressed?
                  main_loop
                                      ; No.
         goto
debounce
         movlw
                    0xff
                                       ; Yes - button was pressed.
                                       ; load a counter to debounce my switch.
                    debounce count
         movwf
```

```
debounce_loop
         btfss PORTB,7 ; Is button released?
goto debounce ; No.
call delay ; Yes. short delay,
decfsz debounce_count ; and decrement counter. Has counter expired?
          goto debounce_loop ; No.
          banksel CLC1POL
          btfss RELAY_CONTROL ; Is relay currently on?
          goto relayon ; No. request turn or goto relayoff ; Yes. request turn off.
                                         ; No. request turn on.
relayon
                RELAY_CONTROL ; raise signal to request relay turn-on.
    goto main_loop
relayoff
                RELAY_CONTROL ; lower signal to request relay turn-off.
    bcf
           main_loop
     goto
delay
    nop
    nop
    return
     end
```

APPENDIX B

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Appendix B contains the CLC configuration file that was generated with the CLC Designer Tool.

ANKSEL	CLCINOPPS	BANKSEL CLC2GLS0
ovlw	H'0E'	movlw H'02'
ovwf	CLCINOPPS	movwf CLC2GLS0
ovlw	H'00'	movlw H'00'
ovwf	CLCIN1PPS	movwf CLC2GLS1
ovlw	н'00'	movlw H'20'
ovwf	CLCIN2PPS	movwf CLC2GLS2
ovlw	H'00'	movlw H'00'
ovwf	CLCIN3PPS	movwf CLC2GLS3
		movlw H'OE'
ANKSEL	CLC1GLS0	movwf CLC2SEL0
ovlw	H'02'	movlw H'00'
ovwf	CLC1GLS0	movwf CLC2SEL1
ovlw	н'00'	movlw H'06'
ovwf	CLC1GLS1	movwf CLC2SEL2
ovlw	H'00'	movlw H'00'
ovwf	CLC1GLS2	movwf CLC2SEL3
ovlw	H'00'	movlw H'00'
ovwf	CLC1GLS3	movwf CLC2POL
ovlw	H'13'	movlw H'81'
ovwf	CLC1SEL0	movwf CLC2CON
ovlw	H'0E'	BANKSEL CLC3GLS0
ovwf	CLC1SEL1	movlw H'02'
ovlw	н'05'	movwf CLC3GLS0
ovwf	CLC1SEL2	movlw H'00'
ovlw	H'00'	movwf CLC3GLS1
ovwf	CLC1SEL3	movlw H'00'
ovlw	H'00'	movwf CLC3GLS2
ovwf	CLC1POL	movlw H'00'
ovlw	H'84'	movwf CLC3GLS3
ovwf	CLC1CON	movlw H'OE'
		movwf CLC3SEL0
		movlw H'04'
		movwf CLC3SEL1
		movlw H'06'
		movwf CLC3SEL2
		movlw H'00'
		movwf CLC3SEL3
		movlw H'02'
		movwf CLC3POL
		movlw H'84'
		movwf CLC3CON

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