dsPIC33F/PIC24H to dsPIC33E/PIC24E Migration and Performance Enhancement Guide

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1.0 INTRODUCTION

This document provides an overview of considerations for migrating from dsPIC33F/PIC24H devices to dsPIC33E/PIC24E devices and includes the section **4.0 "Performance Enhancement Techniques"**.

If you are undertaking this migration, it is recommended that you download data sheets and errata documents for these devices from the Microchip web site (www.microchip.com).

The code developed for dsPIC33F/PIC24H devices can be ported to dsPIC33E/PIC24E devices after making the appropriate changes outlined in this document.

The dsPIC33E/PIC24E devices are based on a new architecture, and feature many improvements and new capabilities over dsPIC33F/PIC24H devices, such as:

- On certain devices, Flash has increased from 256 Kbytes on dsPIC33F/PIC24H devices to 536 Kbytes on dsPIC33E/PIC24E devices, including 24 Kbyte auxiliary Flash program memory
- Maximum operating frequency has increased from 40 MIPS to 60 MIPS @ 125ºC and 70 MIPS @ 85ºC
- On certain devices, RAM has increased from 30 Kbytes on dsPIC33F/PIC24H devices to 52 Kbytes on dsPIC33E/PIC24E
- New Universal Serial Bus (USB) module with On-The-Go (OTG) support
- Auxiliary PLL for USB clock generation
- Larger Interrupt Vector Table (IVT) with more interrupt sources
- Number of direct memory access (DMA) channels increased from 8 to 15
- Peripheral Pin Select (PPS) feature is now available on 64-pin, 100-pin and 144-pin devices
- Enhanced Input Capture module, with number of channels increased from 8 to 16
- Enhanced Output Compare module, with number of channels increased from 8 to 16
- Serial Peripheral Interface (SPI) module with new Enhanced Buffer mode
- New High-Speed Pulse-Width Modulation (PWM) module with up to 7.14 ns resolution for phase, dead time and period

- New 32-bit Quadrature Encoder Interface (QEI) module
- Maximum number of Universal Asynchronous Receiver/Transmitter (UART) modules increased from two to four
- Maximum number of SPI modules increased from two to four
- New 32-bit Cyclic Redundancy Check (CRC) module
- Enhanced Parallel Master Port (PMP) module
- Enhanced Comparator module with three comparators
- Real-Time Clock and Calendar (RTCC) module
- Additional Peripheral Module Disable bits (PMD) are added to disable individual PWM channels and DMA channel groups for power-saving

Note 1: Not all of the features listed previously are available on all devices. Refer to the specific device data sheet for availability.

2: The dsPIC33E/PIC24E devices have been designed to perform to the parameters provided in the respective device data sheets, which are available from the Microchip web site (www.microchip.com), and have been tested to electrical specifications designed to determine their conformance with these parameters.

Due to manufacturing process differences, these devices may have different performance characteristics than their earlier versions. These differences may cause these devices to perform differently in your application than their earlier versions.

For example, the user should verify that the device Oscillator starts and performs as expected. Adjusting the loading capacitor values and/or oscillator mode may be required.

2.0 MIGRATION CONSIDERATIONS SUMMARY

This document discusses several enhancements, changes and application migration considerations related to dsPIC33E/PIC24E devices. Some of the key migration considerations are:

- Operation up to 70 MIPS. Note that the migration to >40 MIPS will affect peripheral clocks and operational characteristics.
- Minor pinout differences and new packages
- Minor instruction set enhancements
- Instruction pipeline differences, resulting in changes to application execution cycle counts
- New Extended Data Space (EDS) addressing and new program space visibility (PSV) access method
- Increased special function register (SFR) space and dual-port RAM, reduced near data memory
- Increased Flash program memory size; changes to Flash access latency
- Increased Run-Time Self-Programming (RTSP) page and row sizes, with changes in methodology; changes in erase/programming times
- Changes to IVT; removed alternate IVT
- Interrupt register changes
- DMA register changes; DMA transfers can now also use non-dual port RAM space
- I/O port analog/digital selection and change notification control register changes
- Peripheral Pin Select (PPS) feature
- Device Configuration register updates
- New peripherals:
  - USB
  - High-Speed PWM
  - 32-bit QEI
  - 32-bit CRC
- Enhanced peripherals:
  - Input Capture
  - Output Compare
  - Analog-to-Digital Converter (ADC)
  - SPI
  - Comparator
  - PMP
- More instantiations of individual peripherals

2.1 Operating Range

The operating frequency of dsPIC33E/PIC24E devices is up to 70 MIPS. The VCAP voltage in dsPIC33E/PIC24E devices is 1.8V, which is provided by an internal voltage regulator.

2.2 Package Migration Considerations

The 64-pin and 100-pin devices of the dsPIC33F/PIC24H and dsPIC33E/PIC24E families are peripheral pin compatible, with the following exceptions:

- I²C™ pin functions, SCL1 and SDA1 (located at pins 57 and 56 on 100-pin dsPIC33F/PIC24H devices), have been relocated to pins 70 and 69 on 100-pin dsPIC33E/PIC24E devices, and renamed to ASCL1 and ASDA1, respectively. These pin functions must be enabled using the ALTI2C1 Configuration bit (FPOR<4>).

  Similarly, on 64-pin dsPIC33E/PIC24E devices, SCL1 and SDA1 have been relocated from pins 37 and 36 to pins 44 and 43, and renamed as ASCL1 and ASDA1.
- I²C pin functions, ASCL2 and ASDA2, which are located at pins 58 and 59 in 100-pin devices. These pins must be enabled using the ALTI2C2 Configuration bit (FPOR<5>). In dsPIC33F/PIC24H devices, pins 58 and 59 contain the SCL2 and SDA2 functions on 100-pin devices.
- I²C pin functions, SCL2 and SDA2 are located at pins 50 and 49 on 100-pin dsPIC33E/PIC24E devices.
- USB pins, which did not exist in dsPIC33F/PIC24H devices
- PMP pins, which did not exist in 64-pin and 100-pin dsPIC33F/PIC24H devices
- Comparator pins, which did not exist in 64-pin and 100-pin dsPIC33F/PIC24H devices
- RTCC pin, which did not exist in 64-pin and 100-pin dsPIC33F/PIC24H devices

The dsPIC33E/PIC24E device families include 121-pin and 144-pin devices.

There are no 80-pin devices in the dsPIC33E/PIC24E device families. Therefore, migrating from an 80-pin dsPIC33F or PIC24H device requires migrating to a different package that is available for dsPIC33E/PIC24E devices, such as 64-pin, 100-pin, 121-pin or 144-pin.

Most digital peripheral pin functions (DCI, SPI, UART, ECAN, Timers, Input Capture, Output Compare, etc.) are remappable in dsPIC33E/PIC24E devices. To migrate from dsPIC33F/PIC24H devices to dsPIC33E/PIC24E devices, these peripherals should be remapped in the software using the Peripheral Pin Select (PPS) feature. Note that certain pins can only be remapped to input peripheral functions, while most other pins can be remapped to either input or output peripheral functions.

For specific details on PPS functionality, refer to the **"I/O Ports"** chapter in the specific device data sheet.

2.3 CPU Architecture and Instruction Set

This section includes the following topics:

- Feature Enhancements
- Instruction Set
- Registers

2.3.1 FEATURE ENHANCEMENTS

The dsPIC33E/PIC24E architecture supports a faster maximum CPU execution speed of 70 MIPS.

The instruction execution pipeline in dsPIC33E/PIC24E devices is different from that of dsPIC33F/PIC24H devices due to a 3-cycle Flash program memory access time. While migrating from a dsPIC33F/PIC24H user application to the dsPIC33E/PIC24E, the program execution times and cycle counts will change. For more details and instruction flow timing diagrams illustrating different instruction flow types, refer to **2.8 "Instruction Flow Types"** in **Section 2.0 "CPU"** (DS70359) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

The PSVPAG register has been replaced by a pair of registers (DSRPAG and DSWPAG), which enables unified support for the new EDS feature as well as the existing PSV access functionality.

2.3.2 INSTRUCTION SET

Note:	For more details on the instruction set, including new instructions, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

Any read operations (including bit operations such as `BSET`/`BCLR`/`BTG`) on peripheral SFRs take two instruction cycles in dsPIC33E/PIC24E devices instead of one instruction cycle.

Program flow change instructions, such as branches and subroutine calls take four instruction cycles in dsPIC33E/PIC24E devices instead of two instruction cycles.

The `RETURN`, `RETFIE`, and `RETLW` instructions require up to six instruction cycles in dsPIC33E/PIC24E devices instead of three instruction cycles.

Besides signed and unsigned multiplications, DSP multiplier-based instructions in dsPIC33E devices also support mixed-sign multiplication operations.

MCU multiplication (`MUL`) instructions in dsPIC33E/PIC24E devices include an option to write the 32-bit multiplication result into Accumulator A or B instead of writing the result to a pair of W registers.

The instruction encoding of the Compare-Skip instructions: CPSEQ, CPSNE, CPSGT and CPSLT, as well as the RCALL Wn and GOTO Wn instructions, has changed in dsPIC33E/PIC24E devices. Ensure that you are using an MPLAB® C30 compiler and MPLAB® IDE version that supports dsPIC33E/PIC24E devices.

The size of the literal value specifying the loop count in DO and REPEAT instructions has been increased from 14 bits to 15 bits in dsPIC33E/PIC24E devices.

The size of the variable (W register) value specifying loop count in DO and REPEAT instructions has been increased from 14 bits to 16 bits in dsPIC33E/PIC24E devices.

The size of the literal value specifying the comparison reference value in the CP and CPB instructions has been increased from 5 bits to 8 bits in dsPIC33E/PIC24E devices.

The number of DO loop nesting levels for which the CPU automatically manages register context save/restore has been increased from one to three in dsPIC33E devices.

The 8-level DO Loop Shadow methodology in the dsPIC33F architecture has been replaced in the dsPIC33E devices with a 4-level DO Loop Hardware Stack. Migrating an application from the dsPIC33F device family will require some changes to user software, if more than four DO loops are being used concurrently in the software. For more details, refer to **2.8 "Instruction Flow Types"** in **Section 2.0 "CPU"** (DS70359) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

On dsPIC33E/PIC24E devices, the first instruction in a DO loop cannot be a PSV read or table read operation.

To support fast literal-value and register writes to the TBLPAG, DSRPAG and DSWPAG registers, the dsPIC33E/PIC24E architecture supports a new base instruction named MOVPAG.

A new base instruction named MULW has been added for dsPIC33E/PIC24E devices. This instruction performs a 16x16 multiplication and generates a 16-bit result.

The new CALL.L instruction allows indirect subroutine calls with 24-bit offsets.

New conditional Compare-Branch instructions: CPBEQ, CPBNE, CPBGT and BPBLT, have been added for dsPIC33E/PIC24E devices.

TBLRDL/TBLRDH instruction requires five instruction cycles in the dsPIC33E/PIC24E devices, unlike dsPIC33F/PIC24H devices, which require two instruction cycles.

2.3.3 REGISTERS

The PSV bit (CORCON<2>) has been replaced by the new Stack Frame Active bit (SFA) in dsPIC33E/PIC24E devices. The SFA status bit, when set, indicates that a stack frame is active, and W14 and W15 will not use EDS.

The US bit (CORCON<12>) has been expanded in dsPIC33E/PIC24E devices to US<1:0> (CORCON<13:12>). When US<1> is clear, the US<0> selections are backward-compatible. Setting US<1:0> to a value of '10' enables the new DSP mixed-sign multiplication mode.

A new bit, VAR (CORCON<15>), has been added in dsPIC33E/PIC24E devices. This bit determines if interrupt processing will use a fixed latency (13 instruction cycles) or variable latency (9 to 13 instruction cycles). For more details on Interrupt Processing Latency, refer to **6.3 "Interrupt Processing Timing"** in **Section 6.0 "Interrupts"** (DS70600) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

The SA bit (SR<13>), SB bit (SR<12>) and SAB bit (SR<10>) need not be cleared manually in software in dsPIC33E/PIC24E devices. Any subsequent instruction that affects these status bits that did not cause a corresponding accumulator saturation condition will clear the bits. In addition, these bits can now be set in software, enabling efficient context state switching.

The DOSTARTH and DOSTARTL registers are read-only in dsPIC33E/PIC24E devices.

2.4 Data Memory

This section includes the following topics:

- Feature Enhancements
- Memory Size and Organization
- Registers

2.4.1 FEATURE ENHANCEMENTS

The dsPIC33E/PIC24E architecture includes a new feature, Extended Data Space (EDS), which is a paged memory scheme used to access RAM addresses greater than 0x7FFF. For more details on EDS usage, refer to **3.2 "Data Space"** in **Section 3.0 "Data Memory"** (DS70595) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

Note 1: On devices with more than 28 Kbytes of RAM, any data objects that may be located at an address greater than 0x7FFF must be assigned a compiler attribute of EDS, as follows:

```
int data[10] __attribute__
((space(ymemory),eds));
```

This includes all Y-RAM and dual-port RAM variables, arrays and pointers.

2: Any user application that uses both PSV accesses and EDS accesses must use the `auto_psv` option of the MPLAB C30 compiler. Assembly language programs must manually adjust the DSRPAG register values to ensure that both PSV and EDS accesses utilize the correct DSRPAG values at all times.

The dsPIC33E/PIC24E devices contain Data Space Arbiter logic to arbitrate concurrent accesses to the same data memory address by the CPU, DMA Controller, USB module and a debugger. Depending on the relative priority assigned by the user to these entities, arbitration can potentially cause some latency in accessing the data. For more details on data space arbitration, refer to **3.2 "Data Space"** in **Section 3.0 "Data Memory"** (DS70595) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

2.4.2 MEMORY SIZE AND ORGANIZATION

The dsPIC33E/PIC24E devices contain up to 52 KB of data RAM, unlike the dsPIC33F/PIC24H devices that have up to 30 KB.

The SFR space has been increased from 2 KB in the dsPIC33F/PIC24H devices to 4 KB in the dsPIC33E/PIC24E devices. This may affect "near" memory mapping, and in some applications, may require reassignment of some data objects in "far" memory. Alternately, the large data model of the MPLAB C30 compiler may be used.

The dsPIC33E/PIC24E devices have 4 KB of Dual-Port RAM, unlike dsPIC33F/PIC24H devices that have up to 2 KB of Dual-Port RAM.

Note: As the stack can be placed in and across x, y and DMA RAM spaces, care must exercised regarding its use, particularly the local automatic variables in a C development environment.

2.4.3 REGISTERS

To support customization of Data Space Arbitration for the specific user application, the dsPIC33E/PIC24E devices have a new register, MSTRPTR. This register can be used by the user software to dynamically assign relative memory access priorities to the CPU, DMA Controller and USB module. By default, the CPU has the highest priority, followed by the USB module and the DMA controller.

Many dsPIC33E/PIC24E SFR addresses have changed relative to the corresponding SFR addresses in the dsPIC33F/PIC24H devices. For precise SFR addresses, refer to the **"Memory Organization"** chapter in the specific device data sheet.

Note: When migrating dsPIC33F/PIC24H software to dsPIC33E/PIC24E, ensure that your application software is using the correct device-specific linker scripts and compiler/assembler include files.

2.5 Flash Program Memory

This section includes the following topics:

2.5.1 FEATURE ENHANCEMENTS

The dsPIC33E/PIC24E devices have some differences in Program Memory organization, the time required to access Program Memory, and the mechanism for accessing constants located in program memory using PSV.

The code execution from primary Flash program memory is not stalled when performing RTSP operations on auxiliary Flash program memory, and code execution from auxiliary Flash program memory is not stalled when performing RTSP operations on primary Flash program memory.

The PSV mechanism to access constants stored in program memory is slightly different in dsPIC33E/PIC24E devices. This access now utilizes the new DSRPAG register instead of the PSVPAG register for generating the read address. The PSV bit and PSVPAG register have been removed in dsPIC33E/PIC24E devices. For specific details about the PSV access mechanism in dsPIC33E/PIC24E devices, refer to **Section 3.0 "Data Memory"** (DS70595) and **Section 4. "Program Memory"** (DS70613) of the "*dsPIC33E/PIC24E Family Reference Manual*".

On dsPIC33E/PIC24E devices, the PSV mechanism can be used to access all the three bytes of a program memory word, unlike dsPIC33F/PIC24H devices where the PSV can only access the lower 16 bits of a program memory word.

PSV accesses now require five instruction cycles, unlike dsPIC33F/PIC24H devices, which require two instruction cycles. There are certain exceptions to this overhead, as described in **Section 2. "CPU"** (DS70359) and **Section 4. "Program Memory"** (DS70613) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

Similar to dsPIC33F/PIC24H devices, dsPIC33E/PIC24E devices also support RTSP. Table 2-1 lists the RTSP differences between the two device families.

2.5.2 MEMORY SIZE AND ORGANIZATION

The dsPIC33E/PIC24E devices contain up to 512 KB of primary Flash program memory, unlike dsPIC33F/PIC24H devices that have up to 256 KB.

The Interrupt Vector Table (IVT) in dsPIC33E/PIC24E devices is twice as large as the IVT in dsPIC33F/PIC24H devices.

There is no Alternate Interrupt Vector Table (AIVT) in dsPIC33E/PIC24E devices.

The dsPIC33E/PIC24E devices include a new 24 KB auxiliary Flash program memory region starting at address 0x7FC000, which can be used for storing constants or executing user code.

2.5.3 REGISTERS

The dsPIC33E/PIC24E devices have a new NVMSIDL bit (NVMCON<12>), which can be used to discontinue the primary and auxiliary Flash program memory operation while the device is in Idle mode.

The ERASE bit (NVMCON<6> in dsPIC33F/PIC24H) has been deleted in dsPIC33E/PIC24E devices.

2.5.4 ELECTRICAL CHARACTERISTICS

Flash program memory erase and programming times in dsPIC33E/PIC24E devices are different from dsPIC33F/PIC24H devices. For Program Memory specifications, refer to **"Electrical Characteristics"** chapter in the specific device data sheet.

Note:	When migrating dsPIC33F/PIC24H software to dsPIC33E/PIC24E devices, ensure that your application software is using the correct device-specific linker scripts and compiler/assembler include files.

2.5.5 RUN-TIME SELF-PROGRAMMING (RTSP)

The RTSP changes between the dsPIC33F/PIC24H and dsPIC33E/PIC24E devices are provided in Table 2-1.

TABLE 2-1: RTSP CHANGES BETWEEN dsPIC33F/PIC24H AND dsPIC33E/PIC24E DEVICES

Parameter	dsPIC33F/PIC24H	dsPIC33E/PIC24E
Smallest program memory page erase size	One page – 512 instructions or 1536 bytes	One page – 1024 instructions or 3072 bytes
Smallest program memory row program size	One row – 64 instructions or 192 bytes	One row – 128 instructions or 384 bytes
Smallest program memory word program size	One word – 1 instruction or 3 bytes	An even-odd pair of words – 2 instructions or 6 bytes
NVMOP<3:0> (NVMCON<3:0>) settings	If ERASE = 1: 1111 = Memory bulk erase operation 1110 = Reserved 1101 = Erase General Segment 1100 = Erase Secure Segment 1011 = Reserved 0011 = No operation 0010 = Memory page erase operation 0001 = No operation 0000 = Erase a single Configuration register byte If ERASE = 0: 1111 = No operation 1110 = Reserved 1101 = No operation 1100 = No operation 1011 = Reserved 0011 = Memory word program operation 0010 = No operation 0001 = Memory row program operation 0000 = Program a single Configuration register byte	1111 = Reserved 1110 = Memory bulk erase operation (primary and auxiliary Flash) 1101 = Bulk erase primary Flash program memory 1100 = Reserved 1011 = Reserved 1010 = Bulk erase auxiliary Flash program memory 0011 = Memory page erase operation 0010 = Memory row program operation 0001 = Memory word program operation 0000 = Program a single Configuration register byte
Location of Program Memory latches for RTSP	Same addresses as the program memory locations to be programmed	Dedicated 128-word latch block located at address 0xFA0000 in Configuration memory space
Method of specifying the program memory row/word or Configuration register to be written by RTSP operation	Destination address of most recent table write instruction defines the row or word to be written	The NVMADRU/NVMADR register (NVM Address) pair must be initialized by user software with the appropriate row /word or Configuration register address

2.6 Interrupt Controller

This section includes the following topics:

- Feature Enhancements
- Memory Size and Organization
- Registers

2.6.1 FEATURE ENHANCEMENTS

New traps have been added in the Interrupt Controller: a generic hard trap at address 0x000008 and a generic soft trap at address 0x000010. Both of these traps can be triggered manually by user software, which provides software traps for debugging or task-switching purposes.

A new NVM Write Complete Interrupt vector has been inserted at address 0x000032 (which was a Reserved vector in the dsPIC33F/PIC24H devices).

Several new interrupt vectors have been added in the previously reserved locations as well as at addresses beyond 0x0000A2, reflecting the new peripheral instances and features present in dsPIC33E/PIC24E devices.

2.6.2 MEMORY SIZE AND ORGANIZATION

The IVT in dsPIC33E/PIC24E devices is twice as large as the IVT in dsPIC33F/PIC24H devices.

There is no AIVT in dsPIC33E/PIC24E devices.

As a result of the insertion of new traps, the addresses of the Stack Error Trap, Math Error Trap and DMA Error Trap vectors have changed to 0x00000A, 0x00000C and 0x00000E, respectively.

The motor control PWM Fault A (FLTA) and Fault B (FLTB) interrupt vectors in dsPIC33F/PIC24H devices have changed to Reserved in dsPIC33E/PIC24E devices.

2.6.3 REGISTERS

Some changes have been made to the Interrupt Request Flag Register (IFSx), Interrupt Enable Register (IECx) and Interrupt Priority Control Register (IPCx) relative to dsPIC33F/PIC24H devices. The locations of the interrupt flag status bits, interrupt enable control bits, and interrupt priority level set bits have been moved across the IFSx, IECx and IPCx registers. For more information on the specifics of these bit locations, refer to the **"Interrupt Controller"** chapter in the specific device data sheet.

The PWM period match interrupt vector has been renamed to PSEM Interrupt in dsPIC33E/PIC24E devices, with corresponding changes in the Interrupt Enable, Interrupt Flag and Interrupt Priority bits.

The QEI interrupt vector has been renamed to QEI1 Interrupt in dsPIC33E/PIC24E devices, with corresponding changes in the Interrupt Enable, Interrupt Flag and Interrupt Priority bit names.

A new bit, VAR (CORCON<15>), has been added in dsPIC33E/PIC24E devices. This bit determines if interrupt processing will use a fixed latency (13 instruction cycles) or variable latency (9 to 13 instruction cycles). For more details on Interrupt Processing Latency, refer to **6.3 "Interrupt Processing Timing"** in **Section 6.0 "Interrupts"** (DS70600) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

The ALTIVT bit (INTCON2<15>) has been replaced by the new Global Interrupt Enable bit (GIE), which allows the user to enable/disable all interrupts without having to explicitly raise the CPU Interrupt Priority in real time.

A new Software Trap Enable (SWTRAP) bit (INTCON2<13>) has been added.

The dsPIC33E/PIC24E devices have a new register, INTCON3, which contains the USB Address Error Soft Trap (UAE), DMA Address Error Soft Trap (DAE) and DO Stack Overflow Soft Trap (DOOVR) status bits.

The dsPIC33E/PIC24E devices have a new register, INTCON4, which contains the Software Generated Hard Trap (SGHT) status bit.

Note:	When migrating dsPIC33F/PIC24H software to dsPIC33E/PIC24E devices, ensure that your application software is using the correct device-specific linker scripts and compiler/assembler include files.

2.7 Direct Memory Access (DMA)

This section includes the following topics:

2.7.1 FEATURE ENHANCEMENTS

On dsPIC33E/PIC24E devices, the DMA Controller can now transfer data from/to any Data RAM address, in addition to the Dual-Port RAM area. Note that accesses of the Dual-Port RAM area are not subject to Data Space Arbitration; therefore, existing DMA transfer latencies observed in a dsPIC33F/PIC24H user application would be maintained when migrating the software to a dsPIC33E/PIC24E device.

The dsPIC33E/PIC24E devices have 15 DMA channels as opposed to eight DMA channels in dsPIC33F/PIC24H devices.

Several new peripheral modules have DMA transfer capability in dsPIC33E/PIC24E devices. These include:

- Timers 4 and 5
- Input Capture channels 3 and 4
- Output Compare channels 3 and 4
- UART modules 3 and 4
- SPI modules 3 and 4
- PMP module (present only in some dsPIC33F/PIC24H devices)

2.7.2 REGISTERS

The IRQSEL<7:0> bits (DMAxREQ<7:0>) include these new peripheral interrupt request (IRQ) selections. Note that all the peripheral modules with DMA support in dsPIC33F/PIC24H devices still have the same IRQ numbers in dsPIC33E/PIC24E devices; therefore, the user software does not need to account for the new peripherals while migrating the existing software from dsPIC33F/PIC24H devices.

The DSADR, DMAxSTA and DMAxSTB registers have been expanded to register pairs (now named DSADRH, DSADRL, DMAxSTAH, DMAxSTAL, DMAxSTBH and DMAxSTBL) in dsPIC33E/PIC24E devices in order to support the increased RAM address range that are now available for DMA transfers. The upper eight bits in the DMAxSTAH and DMAxSTBH registers are not implemented.

Note: The address values to be written to the DMAxSTAH/DMAxSTBH and DMAxSTAL/DMAxSTBL registers can be obtained using these two macros:

```
__builtin_dmapage(&symbol)
__builtin_dmaoffset(&symbol)
```

Both of these macros are described in the *"MPLAB® C Compiler for PIC24 MCUs and dsPIC® DSCs User's Guide"* (DS51284).

The DMACS0 status register has been split into two new registers, DMAPWC and DMARQC, in dsPIC33E/PIC24E devices. The DMAPWC register contains all of the DMA Peripheral Write Collision status bits (PWCOL<14:0>). The DMARQC register contains all of the DMA Request Collision status bits, which have been renamed RQCOL<14:0> in dsPIC33E/PIC24E devices.

The DMACS1 status register has been split into two new registers, DMALCA and DMAPPS, in dsPIC33E/PIC24E devices. The DMALCA register contains the Last Active DMA Channel status bits (LSTCH<3:0>). The DMAPPS register contains the Ping-Pong mode status flags (PPST<14:0>).

2.8 I/O Ports

This section includes the following topics:

2.8.1 FEATURE ENHANCEMENTS

All dsPIC33E/PIC24E devices provide the PPS capability that enables peripheral selection and placement on a wide range of I/O pins, unlike the dedicated pin configuration on 64/80/100-pin dsPIC33F/PIC24H devices. All 18/28/40/44-pin dsPIC33F/PIC24H devices already have the PPS capability.

The PPS configuration feature operates over a fixed subset of I/O pins. The user has to independently map the input and/or output of the remappable peripherals to any of the available remappable pins. Also, note that certain pins can only be mapped to peripheral input functions, whereas many other pins can be mapped to either input or output functions.

For more information on the complete list of peripherals that can be selected using the PPS feature, refer to the device pinout diagrams and refer to the **"I/O Ports"** chapter in the specific device data sheet.

The I/O pins in dsPIC33E/PIC24E devices also feature internal weak pull-down resistors. Instead of a maximum of 24 Change Notification pins, dsPIC33E/PIC24E devices have a Change Notification function associated with every available I/O port pin.

2.8.2 REGISTERS

The IOLOCK SFR bit (OSCCON<6>) and the IOL1WAY Configuration bit (FOSC<5>) have been added in dsPIC33E/PIC24E devices to prevent inadvertent changes to the PPS registers.

The CNEN1, CNEN2, CNPU1 and CNPU2 registers have been replaced by registers CNENA through CNENK, CNPUA through CNPUK, and CNPDA through CNPDK to correspond with the actual port nomenclature, PORTA through PORTK.

The AD1PCFGH, AD1PCFGL, AD2PCFGH and AD2PCFGL registers, which are used for the ANx pins, do not exist in dsPIC33E/PIC24E devices. This functionality is now performed by the ANSELx registers, which are part of the corresponding I/O ports.

2.8.3 ELECTRICAL CHARACTERISTICS

Due to the presence of new peripherals, such as the USB and Comparator, some of the I/O pins that are 5V tolerant on 64-pin and 100-pin dsPIC33F/PIC24H devices, are not 5V tolerant on the corresponding 64-pin and 100-pin dsPIC33E/PIC24E devices:

- 64-pin devices: Pins 4, 5, 6, 8, 35, 54, 55, 60, 61, 62, 63 and 64 are not 5V tolerant on dsPIC33E/PIC24E devices
- 100-pin devices: Pins 10, 11, 12, 14, 55, 83 and 84 are not 5V tolerant on dsPIC33E/PIC24E devices

In addition, there may be changes in the V_{IH}, V_{IL}, V_{OH} and V_{OL} specifications and other electrical characteristics of the I/O pins. Refer to the **"Electrical Characteristics"** chapter of the specific device data sheet for I/O pin input/output specifications. Moreover, when migrating from a dsPIC33F/PIC24H device to a dsPIC33E/PIC24E device, care must be taken to make all supporting circuitry compatible with the source/sink capability of the dsPIC33E/PIC24E device.

2.8.4 PINOUTS

When migrating from a 64-pin dsPIC33F Motor Control device to any 64-pin dsPIC33E/PIC24E device, the following I/O port functions are no longer available:

- RF2 (replaced by USB functions)
- RF6 (replaced by USB functions)

When migrating from a 64-pin dsPIC33F General Purpose device to any 64-pin dsPIC33E/PIC24E device, the following I/O port functions are no longer available:

- RF2 (replaced by USB functions)
- RF6 (replaced by USB functions)
- RG15 (changed to RE5)
- RC1 (changed to RE6)
- RC2 (changed to RE7)

When migrating from a 100-pin dsPIC33F Motor Control device to any 100-pin dsPIC33E/PIC24E device, the following I/O port functions are no longer available:

- RF6 (replaced by USB functions)
- RF7 (replaced by USB functions)

When migrating from a 100-pin dsPIC33F/PIC24H General Purpose device to any 100-pin dsPIC33E/PIC24E device, the following I/O port functions are no longer available:

- RA12 (changed to RE8)
- RA13 (changed to RE9)
- RF6 (replaced by USB functions)
- RF7 (replaced by USB functions)

Note:	On all dsPIC33E/PIC24E devices, the I/O port pins, RG2 and RG3, can only be used as inputs, and only when V_{USB} is applied. There are no LATG2 and LATG3 bits, no Open Drain feature, and no Change Notification weak pull-up/pull-down feature on these two pins.

2.9 Oscillator Configuration

This section includes the following topics:

- Feature Enhancements
- Electrical Characteristics
- Registers

2.9.1 FEATURE ENHANCEMENTS

A new Auxiliary Oscillator and Auxiliary PLL have been added in dsPIC33E/PIC24E devices to provide suitable clock generation for the USB peripheral, which often needs to operate at a frequency unrelated to the system clock.

A new reference clock generator feature and output pin have been added in dsPIC33E/PIC24E devices.

For a detailed explanation and examples on setting up the Oscillator and PLL Control registers for the desired functioning oscillator, refer to the **"Oscillator Configuration"** chapter in the specific device data sheet.

2.9.2 ELECTRICAL CHARACTERISTICS

The primary PLL VCO output range has changed from 100 MHz-200 MHz to 120 MHz-340 MHz.

The maximum system clock frequency (FOSC) permitted has changed from 80 MHz to 140 MHz, reflecting the 70 MIPS capability of the dsPIC33E/PIC24E device family.

2.9.3 REGISTERS

The dsPIC33E/PIC24E-specific differences for the Oscillator registers are summarized in Table 2-2.

TABLE 2-2: SFR DIFFERENCES FOR dsPIC33E/PIC24E OSCILLATOR

SFR	Differences from dsPIC33F/PIC24H	Data Sheet Chapter
OSCCON	A new bit named IOLOCK has been added to the OSCCON register, to lock the PPS register from changes.	**"Oscillator Configuration"**
ACLKCON2	New register added in dsPIC33E/PIC24E devices to configure the auxiliary PLL.	
ACLKDIV2	New register added in dsPIC33E/PIC24E devices to configure the auxiliary PLL.	
REFOCON	New register added in dsPIC33E/PIC24E devices to configure the oscillator reference output.	

2.10 Reset

This section includes the following topics:

- Registers
- Electrical Characteristics

2.10.1 REGISTERS

A new VREGSF bit (RCON<13>) has been added in dsPIC33E/PIC24E devices. This bit, when set, enables the user application to power down the Flash program memory when the device is in Sleep mode.

The VREGS bit (RCON<8>) is present in dsPIC33E/PIC24E devices; however, some dsPIC33F/PIC24H devices do not have this bit.

The CM bit (RCON<9>) is present in dsPIC33E/PIC24E devices; however, some dsPIC33F/PIC24H devices do not have this bit.

Several SFR reset values have changed relative to the dsPIC33F/PIC24H devices, mainly as a result of the SFR bit changes. To determine the exact default value of each SFR used by the application, refer to the specific device data sheet. While porting application software from dsPIC33F/PIC24H devices, it is highly recommended to explicitly initialize every relevant SFR instead of assuming the default states.

2.10.2 ELECTRICAL CHARACTERISTICS

The BOR voltage limits have changed relative to dsPIC33F/PIC24H devices.

2.11 Power-Saving Modes

2.11.1 REGISTERS

In dsPIC33E/PIC24E devices, the DOZE bits can only be written to when the DOZEN bit (CLKDIV<11>) is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored. Also, the DOZEN bit cannot be set, if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by the user software to set the DOZEN bit is ignored.

The PMD3 register in dsPIC33E/PIC24E devices has the CMPMD, RTCCMD, PMPMD and CRCMD bits; however, some dsPIC33F/PIC24H devices do not have these bits.

PMD3<4> is now the U3MD bit.

New registers PMD4 to PMD7 have been added, reflecting the enhanced peripheral set in dsPIC33E/PIC24E devices.

For the SFR details, refer to the specific device data sheet.

2.12 Timers

The functionality of Timer1 through Timer9 in dsPIC33E/PIC24E devices is identical to dsPIC33F/PIC24H devices, except that writes to the TMR1 register are ignored in External Synchronous Counter mode, if Timer1 is enabled.

Note:	When configured as a counter, the timer pins must be mapped to the appropriate I/O pins using the PPS feature.

2.12.1 FEATURE ENHANCEMENTS

Timer2, 3, 4 or 5 can also be used as the time base for the Input Capture and Output Compare channels, unlike dsPIC33F/PIC24H devices, which can only use Timer2 or Timer3 for this purpose.

Also, in addition to Timer2 and Timer3, dsPIC33E/PIC24E devices also support DMA transfers from Timer4 and Timer5.

2.13 Input Capture

This section includes the following topics:

- Feature Enhancements
- Registers

The dsPIC33E/PIC24E devices contain up to 16 Input Capture channels, unlike the maximum of eight Input Capture channels provided by dsPIC33F/PIC24H devices.

Note:	The Input Capture pins must be mapped to the appropriate I/O pins using the PPS feature.

Moreover, in addition to Input Capture channels 1 and 2, dsPIC33E/PIC24E devices also support DMA transfers from Input Capture channels 3 and 4.

2.13.1 FEATURE ENHANCEMENTS

Timer1 through Timer5 can now be used as the time base for any Input Capture channel.

Alternatively, the system clock can also be the time base for any Input Capture channel.

An even/odd pair of Input Capture timers can be used in a concatenated 32-bit configuration, which is known as Cascaded mode.

Triggered mode, where any Input Capture channel can be held in its reset state until it receives a trigger signal from any of the following peripheral modules:

- Timer1 through Timer5
- ADC1 module
- Comparator 1 through Comparator 3
- Input Capture channels 1 to 9
- Output Compare channels 1 to 9

Synchronized mode, where any Input Capture channel can be reset when it receives a synchronizing signal from any of the following peripheral modules:

- Timer1 through Timer5
- ADC1 module
- Comparator 1 through Comparator 3
- Input Capture channels 1 to 9
- Output Compare channels 1 to 9

2.13.2 REGISTERS

The dsPIC33E/PIC24E-specific differences for the Input Capture registers are summarized in Table 2-3.

TABLE 2-3: SFR DIFFERENCES FOR dsPIC33E/PIC24E INPUT CAPTURE

SFR	Differences from dsPIC33F/PIC24H	Data Sheet Chapter
ICxCON1	The ICxCON register in dsPIC33F/PIC24H devices has been renamed as ICxCON1 in dsPIC33E/PIC24E devices. The following bits have changed: • The ICTMR bit (ICxCON1<7>) has been relocated and renamed as ICTSEL<2:0> (ICxCON1<12:10>) • The ICTSEL<2:0> bit selections have changed to include Timer1 through Timer5 and the system clock (TCY) as possible Input Capture timebases	**"Input Capture"**
ICxCON2	New register in the dsPIC33E/PIC24E devices, which contains the IC32, ICTRIG, TRIGSTAT and SYNCSEL<4:0> bits to enable and configure the new Trigger, Synchronization and Cascaded modes. This register must be explicitly initialized even if these new features are not being used.	

2.14 Output Compare

This section includes the following topics:

2.14.1 FEATURE ENHANCEMENTS

The dsPIC33E/PIC24E devices contain up to 16 Output Compare channels, unlike the maximum of eight Output Compare channels provided by dsPIC33F/PIC24H devices.

Note:	The Output Compare pins must be mapped to the appropriate I/O pins using the PPS feature.

In addition to the Output Compare channels 1 and 2, dsPIC33E/PIC24E devices also support DMA transfers from Output Compare channels 3 and 4.

Each Output Compare channel in dsPIC33E/PIC24E devices contains several new features.

Timer1 through Timer5 can now be used as the timebase for any Output Compare channel.

Alternatively, the system clock can also be the time base for any Output Compare channel.

The dsPIC33E/PIC24E devices support Cascaded mode, where an even/odd pair of Output Compare timers can be used in a concatenated 32-bit configuration.

The dsPIC33E/PIC24E devices support Triggered mode, where any Output Compare channel can be held in its reset state until it receives a trigger signal from any of the following peripheral modules:

- Timer1 through Timer5
- ADC1 module
- Comparator 1 through Comparator 3
- Input Capture channels 1 to 9
- Output Compare channels 1 to 9

The dsPIC33E/PIC24E devices support Synchronized mode, where any Output Compare channel can be reset when it receives a synchronizing signal from any of the following peripheral modules:

- Timer1 through Timer5
- ADC1 module
- Comparator 1 through Comparator 3
- Input Capture channels 1 to 9
- Output Compare channels 1 to 9

Optional polarity inversion or tri-stating of each Output Compare pin is supported in dsPIC33E/PIC24E devices.

The dsPIC33E/PIC24E devices have three Output Compare Fault pins, OCFA, OCFB and OCFC:

- Any of the 16 Output Compare channels can use one or more of the three Fault pins, unlike dsPIC33F/PIC24H devices, which have two dedicated Fault pins (OCFA for Output Compare channels 1 to 4 and OCFB for Output Compare channels 5 to 8).
- Cycle-by-Cycle and latched Fault modes
- Configurable Output Compare pin state on a Fault event
- Optional tri-stating of PWM output on a Fault event

2.14.2 REGISTERS

The dsPIC33E/PIC24E-specific changes made to the Output Compare registers are summarized in Table 2-4.

TABLE 2-4: SFR CHANGES FOR dsPIC33E/PIC24E OUTPUT COMPARE

SFR	Differences from dsPIC33F/PIC24H	Data Sheet Chapter
OCxCON1	The OCxCON register in dsPIC33F/PIC24H has been renamed as OCxCON1 in dsPIC33E/PIC24E devices and the following bits have changed: • The OCTSEL bit (OCxCON<3>) from dsPIC33F/PIC24H devices has been relocated and expanded to OCTSEL<2:0> (OCxCON1<12:10>) • The OCTSEL<2:0> bit selections have changed to include Timer1 through Timer5 and the system clock as possible Input Capture timebases • The OCFLT bit (OCxCON<4>) from dsPIC33F/PIC24H devices has been removed • New ENFLTC, ENFLTB and ENFLTA control bits (OCxCON1<9:7>) to enable individual faults • New OCFLTC, OCFLTB and OCFLTA status bits (OCxCON1<6:4>) to indicate individual fault conditions • New Trigger Status Mode Select bit, (TRIGMODE) bit (OCxCON1<3>) • The mode selections for OCM<2:0> = 110 and 111 (OCxCON1<2:0>) have changed in dsPIC33E/PIC24E devices	**"Output Compare"**
OCxCON2	New register in dsPIC33E/PIC24E devices that contains the FLTMD, FLTOUT, FLTTRIEN, OCINV, OC32, OCTRIG, TRIGSTAT, OCTRIS and SYNCSEL<4:0> bits to enable and configure the new Trigger, Synchronization, and Cascaded modes, as well as other new features listed previously. This register must be explicitly initialized even if these new features are not being used.	
OCxRS(1)	This register is used to specify the period in PWM mode in the dsPIC33E/PIC24E devices, whereas in dsPIC33F/PIC24H devices, it is used to specify the duty cycle in PWM mode.	
OCxR(1)	This register is used to specify the duty cycle in PWM mode in dsPIC33E/PIC24E devices, whereas in dsPIC33F/PIC24H devices, this register is unused in PWM mode.	

Note 1: The OCxRS and OCxR registers are double-buffered in dsPIC33E/PIC24E devices.

2.15 High-Speed PWM

The new High-Speed PWM module in dsPIC33E/PIC24E devices is substantially more advanced than the Motor Control PWM module in dsPIC33F devices, with a new enhanced set of SFRs and associated control and status bits.

Note: The Motor Control PWM module is not available in PIC24H devices.

In addition to the PWM features provided by dsPIC33F devices, the dsPIC33E/PIC24E High-Speed PWM module provides several additional enhancements and new features:

- Up to seven PWM generators, with two PWM outputs per generator
- Individual time base and duty cycle for each PWM output
- Primary and secondary master time base to support dual 3-phase motor control
- Maximum PWM clock input of 2 * FCY instead of 40 MHz
- Duty cycle, dead time, phase shift and frequency resolution of 7.14 ns at 70 MIPS
- Independent fault and current-limit inputs for up to 14 PWM outputs
- Redundant Output mode
- True Independent Output mode
- Output override control
- Special event trigger
- PWM capture
- Multiple triggers from PWM to ADC per PWM period
- Independent PWM frequency, duty cycle and phase shift changes
- Leading Edge Blanking (LEB)
- Complementary mode
- Push-Pull mode
- Edge-Aligned mode
- Center-Aligned PWM mode
- Multi-Phase mode
- Variable Phase mode
- Fixed Off-Time mode
- Current Reset mode
- Current-Limit mode
- Dead-time compensation feature – an enhancement to the dead-time insertion feature

Note 1: The PWM synchronization, fault and dead time compensation pins must be mapped to the appropriate I/O pins using the PPS feature.

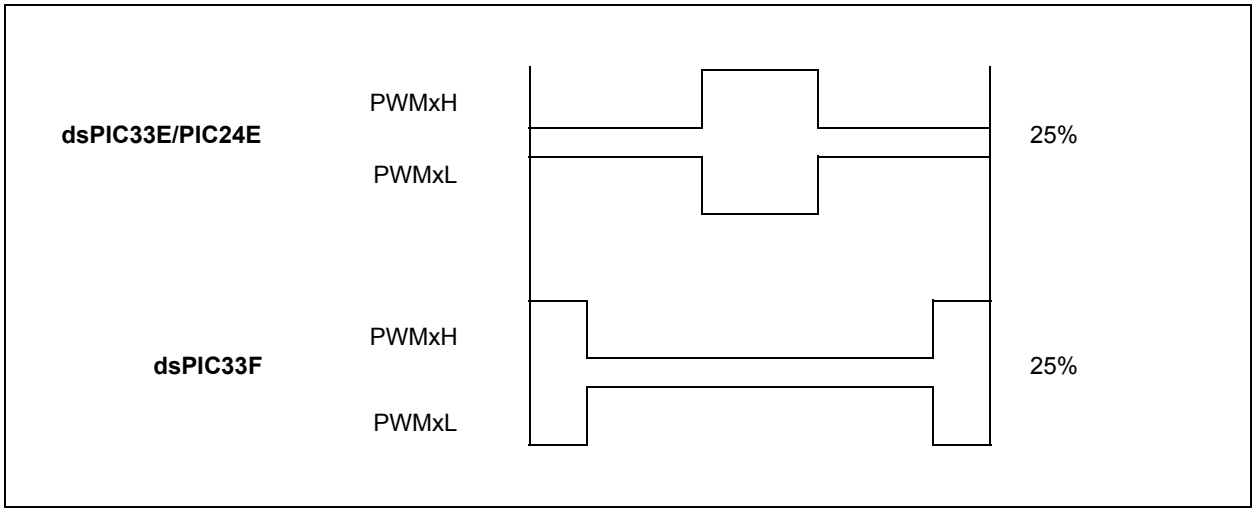
2: In Center-Aligned mode, dsPIC33E/PIC24E devices have the positive duty cycle centered at the mid-point of the PWM period, while in dsPIC33F devices the duty cycle is centered in the beginning and end of the PWM period (see Figure 2-1).

3: The double-update feature for duty cycle updates is not available in dsPIC33E/PIC24E devices.

4: There is no Special Event Counter Direction bit (SEVTDIR) or the PWM Direction bit (PTDIR) in dsPIC33E/PIC24E devices.

For a detailed description of this module, refer to **Section 14. "High-Speed PWM"** (DS70645) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

FIGURE 2-1: CENTER-ALIGNED MODE DIFFERENCE BETWEEN dsPIC33F AND dsPIC33E/PIC24E PWM



2.16 Quadrature Encoder Interface (QEI)

The dsPIC33E devices have up to two 32-bit QEI modules. These new modules are substantially more advanced than the dsPIC33F 16-bit QEI module, with a new enhanced set of SFRs and associated control and status bits. The new features are:

- 32-bit Position Counter (expanded from 16-bit in dsPIC33F devices)
- New HOME input pin for homing signals
- New 32-bit Initialization/Capture register and QEI Capture feature
- New 32-bit Index Counter
- New 32-bit Greater Than or Equal Compare register
- New 32-bit Less Than or Equal Compare register
- New 32-bit Interval Timer
- New 16-bit Velocity Counter
- Module enable/disable control
- Four different modes for Multiple Index Match
- Several different events can initialize the Position Counter
- Eight input clock prescaler options instead of four
- 4x count resolution only (no 2x mode)
- Polarity control and optional swapping of pins
- Programmable digital filters on input pins
- Separate status flags for distinct interrupt events

Note:	The QEI pins must be mapped to the appropriate I/O pins using the PPS feature.

For a detailed description of this module, refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

2.17 Analog-to-Digital Converter (ADC)

This section includes the following topics:

- Feature Enhancements
- Registers

The dsPIC33E/PIC24E devices have up to two ADC modules.

The ADC1 module in dsPIC33E/PIC24E devices is similar in overall functionality to that in dsPIC33F/PIC24H devices. However, the ADC2 module in dsPIC33E/PIC24E devices only supports the 10-bit operating mode.

2.17.1 FEATURE ENHANCEMENTS

Additional sources of conversion triggers are available in dsPIC33E/PIC24E devices as compared to dsPIC33F/PIC24H devices.

The ADC1 module in dsPIC33E/PIC24E devices supports scanning of up to 32 analog input channels, unlike dsPIC33F/PIC24H devices, which support scanning of up to 16 channels.

Unlike the dsPIC33F/PIC24H ADC module, which included either a 16-word result buffer in SFR space or DMA support (depending on the device) but not both, dsPIC33E/PIC24E devices provide users with the option of either using a 16-word buffer in SFR space or using DMA for storing conversion results in dual-port or single-port RAM.

Note:	The AD1PCFGH, AD1PCFGL and AD2PCFGL registers, used for analog/digital configuration for the ANx pins, have been deleted in dsPIC33E/PIC24E devices. This function is now performed by the ANSELx registers, which are part of the corresponding I/O ports.

2.17.2 REGISTERS

The dsPIC33E/PIC24E-specific differences for the ADC registers are summarized in Table 2-5.

TABLE 2-5: SFR CHANGES FOR dsPIC33E/PIC24E ADC MODULE

SFR	Differences from dsPIC33F/PIC24H	Data Sheet Chapter
ADxCON1	The ADxCON1 SFR changes are: • The AD2CON1 SFR does not contain the AD12B bit (ADxCON1<10>) in dsPIC33E/PIC24E devices • New SSRCG bit (ADxCON1<4>) selects between two alternate sets of conversion trigger sources • If SSRCG = 1, the SSRC<2:0> bits (ADxCON1<7:5>) can be used to select any of the individual PWM Generators 1 to 7 as conversion trigger sources • If SSRCG = 0, setting SSRC<2:0> = 011 selects the PWM Primary Special Event Trigger as the conversion trigger and setting SSRC<2:0> = 101 selects the PWM Secondary Special Event trigger • If SSRCG = 0, setting SSRC<2:0> = 010 and 100 select Timer3 and Timer5, respectively on both the ADC1 and ADC2 modules	**"10-bit/12-bit Analog-to-Digital Converter (ADC)"**
ADxCON2	In the ADC1 module, the SMPI<3:0> bits (AD1CON2<5:2>) have been expanded to SMPI<4:0> (AD1CON2<6:2>).	
ADxCON3	The ADCS<7:0> bits (ADxCON3<7:0>) allow selection of TAD values up to 256 * TCY in dsPIC33E/PIC24E devices. In dsPIC33F/PIC24H devices, selections greater than 64 * TCY are reserved.	
ADxCON4	The new ADDMAEN bit (ADxCON4<8>) provides the user the option to either use DMA or a 16-word deep buffer in SFR space for storing conversion results. Depending on whether DMA is enabled or not, the interpretation of the SMPI<4:0> bits will vary.	

2.18 Universal Asynchronous Receiver/Transmitter (UART)

2.18.1 FEATURE ENHANCEMENTS

The only UART related change in dsPIC33E/PIC24E devices relative to dsPIC33F/PIC24H devices is the increase in the number of UART modules from two to four. Also, all four UART modules have DMA support in dsPIC33E/PIC24E devices.

Note:	The UART pins must be mapped to the appropriate I/O pins using the PPS feature.

2.19 Inter-Integrated Circuit™ (I^2C™)

2.19.1 FEATURE ENHANCEMENTS

There is no change in the functionality or number of I^2C modules in dsPIC33E/PIC24E devices relative to dsPIC33F/PIC24H devices, except for the addition of alternate I^2C pins.

Note:	The ALTI2C1 and ALTI2C2 bits in the FPOR Configuration register must be configured correctly, especially when migrating dsPIC33F/PIC24H applications to dsPIC33E/PIC24E devices.

2.20 Serial Peripheral Interface (SPI)

This section includes the following topics:

- Feature Enhancements
- Registers

2.20.1 FEATURE ENHANCEMENTS

The number of SPI modules in dsPIC33E/PIC24E devices has increased from two to four. Also, all four SPI modules in dsPIC33E/PIC24E devices have DMA support.

In addition, each SPI module in dsPIC33E/PIC24E devices supports Enhanced Buffer mode, which uses an 8-word deep hardware Transmit/Receive FIFO Buffer.

Note 1:	Certain devices have at least one SPI module that uses dedicated pins and can achieve higher speeds. See the specific device data sheet to determine whether an SPI module is available on dedicated pins.
2:	The SPI pins must be mapped to the appropriate I/O pins using the PPS feature.

2.20.2 REGISTERS

The dsPIC33E/PIC24E-specific differences for the SPI registers are summarized in Table 2-6.

TABLE 2-6: SFR DIFFERENCES FOR dsPIC33E/PIC24E SPI MODULE

SFR	Differences from dsPIC33F/PIC24H	Data Sheet Chapter
SPIxCON1	PPRE<1:0> and SPRE<2:0> settings of '11' and '111' are Reserved in the dsPIC33E/PIC24E devices.	**"Serial Peripheral Interface (SPI)"**
SPIxCON2	New SPIBEN bit (SPIxCON2<0>) is used to enable/disable Enhanced Buffer mode.	
SPIxSTAT	SPIxSTAT SFR changes: • In Enhanced Buffer mode, the SPITBF or SPIRBF bits (SPIxCON2<1:0>) get set only when the entire Transmit/Receive FIFO buffer is full • New SPIBEC<2:0> (SPIxSTAT<10:8>), SRMPT (SPIxSTAT<7>) and SRXMPT (SPIxSTAT<5>) status bits specific to Enhanced Buffer mode • New SISEL<2:0> control bits (SPIxSTAT<4:2>) to specify the buffer interrupt mode in Enhanced Buffer mode	

2.21 Data Converter Interface (DCI)

There is no change in the functionality or number of DCI modules in dsPIC33E/PIC24E devices relative to dsPIC33F/PIC24H devices.

Note:	The DCI pins must be mapped to the appropriate I/O pins using the PPS feature.

2.22 Enhanced CAN (ECAN™)

There is no change in the functionality or number of ECAN modules in dsPIC33E/PIC24E devices relative to dsPIC33F/PIC24H devices.

Note:	The ECAN pins must be mapped to the appropriate I/O pins using the PPS feature.

2.23 Universal Serial Bus (USB)

The USB OTG module in dsPIC33E/PIC24E devices is a new communication peripheral module that is not present in dsPIC33F/PIC24H devices. For a detailed description of this module, refer to **Section 25. "USB On-The-Go (OTG)"** (DS70571) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

2.24 Comparator

This section includes the following topics:

- Feature Enhancements
- Registers

2.24.1 FEATURE ENHANCEMENTS

The Comparator module in dsPIC33E/PIC24E devices includes several enhancements relative to the Comparator module in 28-pin, 40-pin and 44-pin dsPIC33F/PIC24H devices.

The number of comparators have increased from two to three in dsPIC33E/PIC24E devices. The comparator input pins are now named as CxINA, CxINB, CxINC and CxIND (x = 1, 2 or 3).

The dsPIC33E/PIC24E devices provide a new Blanking Function feature configured using two new registers, CxMSKSRC and CxMSKCON.

For a detailed description of the Blanking Function and these registers, refer to **Section 26. "Comparator"** (DS70357) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

The dsPIC33E/PIC24E devices provide a new Filter feature to prevent glitches and unwanted comparator transitions. The Comparator Filter clock selection and period are configured using the new register, CMxFLTR.

The dsPIC33E/PIC24E devices provide the ability to control the low-power mode operation of each Comparator by setting the CLPWR bit (CMxCON<12>).

The dsPIC33E/PIC24E devices provide multiple Trigger/Event/Polarity configurations, selected using the EVPOL<1:0> bits (CMxCON<7:6>).

The dsPIC33E/PIC24E devices provide new Band-Gap Reference Source options (0.2V, 0.6V or 1.2V) for the non-inverting input. This is selected using the new BGSEL<1:0> bits (CVRCON<9:8>).

The new VREFSEL bit (CVRCON<10>) provides an additional Voltage Reference selection, a 4-bit internal resistor network output (VREFSEL = 0).

Note:	The Comparator output pins must be mapped to the appropriate I/O pins using the PPS feature.

2.24.2 REGISTERS

The CMSIDL control bit, as well as the CxEVT and CxOUT status bits, have been relocated to a new register, CMSTAT.

Each Comparator now has its own control register named CMxCON, which includes the following bits:

- Comparator Enable bit (renamed as CON)
- Comparator Output Enable bit (renamed as COE)
- Comparator Polarity bit (renamed as CPOL)
- Comparator Event status bit (renamed as CEVT)
- Comparator Output bit (renamed as COUT)
- Comparator Channel selection bits (renamed as CCH<1:0>)
- Comparator Reference selection bits (renamed as CREF)

2.25 32-bit Cyclic Redundancy Check (CRC)

This section includes the following topics:

- Feature Enhancements
- Registers

2.25.1 FEATURE ENHANCEMENTS

The 32-bit CRC module in dsPIC33E/PIC24E devices includes several enhancements relative to the 16-bit CRC module on 28-pin, 40-pin and 44-pin dsPIC33F/PIC24H devices.

2.25.2 REGISTERS

The CRCDAT, CRCXOR and CRCWDAT registers are 32-bit register pairs in dsPIC33E/PIC24E devices (CRCDATH/CRCDATL, CRCXORH/CRCXORL and CRCWDATH/CRCWDATL).

The CRCCON register in dsPIC33F/PIC24H devices has been replaced by two registers, CRCCON1 and CRCCON2, in dsPIC33E/PIC24E devices.

The new LENDIAN bit (CRCCON1<3>) allows the data to be optionally shifted into the CRC Engine Least Significant Bytes (LSB) first.

The new CRCEN bit (CRCCON1<15>) enables the CRC module.

The new CRCISEL bit (CRCCON1<5>) defines whether the interrupt occurs when the FIFO becomes empty or when the CRC result is available.

The new DWIDTH<4:0> bits (CRCCON2<11:8>) enable the user to configure the width of the data word.

The PLEN<3:0> bits in dsPIC33F/PIC24H devices have been expanded to PLEN<4:0> and moved to CRCCON2<4:0> in dsPIC33E/PIC24E devices.

2.26 Parallel Master Port (PMP)

This section includes the following topics:

- Feature Enhancements
- Registers

2.26.1 FEATURE ENHANCEMENTS

The PMP module in dsPIC33E/PIC24E devices includes some enhancements relative to the PMP module in 28-pin, 40-pin and 44-pin dsPIC33F/PIC24H devices.

The number of address lines have been increased from 12 (PMA<14>:PMA<10:0>) to 16 (PMA<15:0>) in dsPIC33E/PIC24E devices.

The number of Chip Select lines have been increased from one (PMCS1 only) to two (PMCS1 and PMCS2).

2.26.2 REGISTERS

The CSF<1:0> bit (PMCON<7:6>) field selections have been enhanced to include both PMCS1 and PMCS2 as possible Chip Select lines.

A new bit named CS2P (PMCON<4>) controls the polarity of the Chip Select 2 signal.

The PMADDR register has all 16 bits implemented in dsPIC33E/PIC24E devices, with PMADDR<15> and PMADDR<14> being the CS2 and CS1 Chip Select bits, respectively.

The PMAEN register has all 16 bits implemented in dsPIC33E/PIC24E devices, with PMAEN<13:11> being PTEN<13:11> and PMAEN<15> being the PMCS2 Strobe Enable bit.

2.27 Real-Time Clock and Calendar (RTCC)

There is no change in the functionality or number of RTCC modules in dsPIC33E/PIC24E devices relative to the 28-pin and 40-pin dsPIC33F/PIC24H devices that include this module.

2.28 CodeGuard™ Security

This section includes the following topics:

- Feature Enhancements
- Registers

The dsPIC33E/PIC24E devices include basic code security for the primary Flash program memory and auxiliary Flash program memory.

2.28.1 FEATURE ENHANCEMENTS

New auxiliary Flash program memory code protection features, including the AWRP, APL and APLK<1:0> bits located in the new FAS configuration register have been added.

2.28.2 REGISTERS

No Boot Segment or Secure Segment (that is, there is no FBS or FSS configuration register in dsPIC33E/PIC24E devices).

No RAM security (that is, there is no BSRAM or SSRAM SFR in dsPIC33E/PIC24E devices).

The GSS<1> bit in the FGS configuration register is not implemented, as GSS is now a single bit in dsPIC33E/PIC24E devices.

The new GSSK<1:0> bits (FGS<5:4>) add an additional layer of protection for the FGS configuration register.

2.29 Programming and Diagnostics

There is no change in either the Joint Test Action Group (JTAG) boundary-scan functionality or in the basic communication interface used for programming the devices.

However, there are some changes in the specifics of the In-Circuit Serial Programming™ (ICSP™) and Enhanced ICSP techniques and programming algorithms, as well as in the JTAG ID details. For more details, refer to the *"dsPIC33E/PIC24E Flash Programming Specification"* (DS70619).

The dsPIC33E/PIC24E devices provide enhanced debugging features. For more details, refer to the MPLAB Help files.

2.30 Device Configuration Registers

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped starting at program memory location 0xF80004.

The Configuration registers, which have changed relative to dsPIC33F/PIC24H devices are:

- General Segment Code Security (FGS)
- Oscillator Control (FOSC)
- Power-on Reset Configuration (FPOR)
- In-Circuit Debugger Configuration (FICD)
- Auxiliary Flash Program Memory Security (FAS)
- User Unit ID (FUID0)

The changes in the device configuration registers are listed in Table 2-7, except for the changes to the FGS and FAS configuration registers, which are outlined in **Section 2.28 "CodeGuard™ Security"**.

For more information on the specifics of new registers and changes to the existing registers, refer to the **"Special Features"** chapter in the specific device data sheet.

TABLE 2-7: DEVICE CONFIGURATION REGISTER CHANGES FOR dsPIC33E/PIC24E

Address	Register	Differences from dsPIC33F/PIC24H	Data Sheet Chapter
0xF80008	FOSC	The PPS Configuration bit (IOL1WAY) has been added (FOSC<5>). The IOL1WAY bit allows a single or multiple PPS reconfiguration.	**"Special Features"**
0xF8000C	FPOR	• The BOREN bit, which enables and disables the BOR feature, has been added to the Power-on Reset register (FPOR) • The Alternate I2C1 and I2C2 pin select bits (ALTI2C1 and ALTI2C2) have also been added to the FPOR register • The PWMPIN, HPOL and LPOL bits (present in dsPIC33F Motor Control device families only) have been removed in the dsPIC33E Motor Control device family	
0xF8000E	FICD	New RSTPRI bit added to the FICD register. This bit, when '0', causes the device to execute code from the auxiliary Flash program memory on Reset.	
0xF80012	FUID0	Unlike dsPIC33F/PIC24H devices that had four Unit ID configuration registers at 0xF80010, 0xF80012, 0xF80014 and 0xF80016, dsPIC33E/PIC24E devices have a single Unit ID configuration register at address 0xF80012.	

3.0 ADDITIONAL DEVICE DIFFERENCES

This section specifies additional device differences to consider while migrating between the devices listed in Table 3-1. All of the previously mentioned migration considerations presented in this guide are still applicable with the exception of specific features that are not available (i.e., USB, Ethernet, etc.).

3.1 Package/Pinout Considerations

Many pin functions have changed between these families of devices. It is recommended that you download the specific device data sheets and errata documents from www.microchip.com and thoroughly review the pin diagrams for each device.

TABLE 3-1: DEVICE DIFFERENCES

Feature	Device Families	
	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X	**dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 PIC24HJ32GP202/204 and PIC24HJ16GP304**
Flash	Up to 256 KB	Up to 32 KB
RAM	Up to 32 KB	2 KB
Device Configuration Registers	Configuration bits are stored in program memory space.	Configuration bits are stored in configuration memory space.
Internal Fast RC (FRC) Oscillator	7.3728 MHz <±0.9% from -40°C to +85°C and 3.0V < VDD < 3.6V 7.3728 MHz <±2% from -40°C to +125°C and 3.0V < VDD < 3.6V	7.3728 MHz ±2% from -40°C to +85°C and 3.0V < VDD < 3.6V 7.3728 MHz ±5% from -40°C to +125°C and 3.0V < VDD < 3.6V
Internal Low-Power RC (LPRC) Oscillator	32.768 kHz ±15% from -40°C to +85°C 32.768 kHz ±30% from -40°C to +125°C	32.768 kHz ±20% up to 85°C 32.768 kHz ±70% up to 125°C
Secondary Oscillator	This feature is not available in these devices.	Secondary Oscillator (Sosc).
Peripheral Pin Select (PPS)	Up to 17 bidirectional remappable pins and up to 37 remappable inputs	Up to 16 bidirectional remappable pins.
Charge Time Measurement Unit (CTMU)	mTouch™ Capacitive Sensing provides high-resolution time measurement and on-chip temperature measurement capability.	This feature is not available in these devices.
Peripheral Trigger Generator (PTG)	Provides the ability to schedule complex peripheral operations. Can trigger peripherals such as Output Compare, Input Capture, Op Amp/ Comparator, ADC, and PWM.	This feature is not available in these devices.
Op amp/Comparator	Three comparators that can be configured as Op amps. One dedicated comparator. Multiple input sources. Blanking and filtering options. Internal or external voltage references.	This feature is not available in these devices.
Windowed Watchdog Timer (WDT)	Four available windowed WDT options.	Single windowed WDT option.

4.0 PERFORMANCE ENHANCEMENT TECHNIQUES

As with any microcontroller, there are various techniques that can be utilized by code developers to improve the performance of an application. This section will explore how to take advantage of the dsPIC33E/PIC24E architectural features to enhance the performance of a user application and increase the effective bandwidth of the CPU.

This section includes the following topics:

- Code Constant Storage
- C Compiler Optimization Options
- Coding Guidelines

4.1 Code Constant Storage

Whenever possible, always place data constants in RAM instead of Flash memory.

4.1.1 FLASH VERSUS RAM VARIABLE STORAGE

PSV and Flash data constant access can take up to five instruction cycles compared to one for data RAM accesses. If certain Flash constants are frequently accessed, or the application has large-to-medium segments of constant tables that are being accessed, if feasible, consider placing them in RAM instead of Flash.

Note:	DSP constants, such as FFT coefficients that may be placed in Flash by the user, are automatically handled by the DSP library functions. The DSP library functions, when appropriate, copy Flash data into the RAM stack space during execution, resulting in higher performance. No user intervention is normally required, although the process can be tuned by the user for maximum performance. Refer to the **"Stack Guard Function"** in the DSP Library Help for more information.

4.1.2 RAM SIZE LIMITATIONS

If there is insufficient RAM to hold large Flash constant value tables, consider using the `REPEAT` instruction with the indirect auto increment move instruction to copy smaller segments of Flash data into a user-defined scratch pad RAM area for application access (see Example 4-1). Repeat copy instructions will execute two and a half times faster than normal Flash read accesses. Copying Flash data into RAM utilizing this technique for segments larger than approximately 20 words will yield positive performance boosts. The larger the data segment being copied into RAM, the larger the performance gains.

EXAMPLE 4-1:

```
__psv__ __attribute__((space(auto_psv))) unsigned int my_constants[10];  //Flash data constants

unsigned int my_scratchpad[10];                          //Scratch pad ram area
unsigned int *p = my_scratchpad;                         //Scratch pad pointer

int main(void)
{
  DSRPAG = (int) __builtin_psvpage(&my_constants);       //dsPIC33E family - select psv page
  //PSVPAG = (int) __builtin_psvpage(&my_constants);     //dsPIC33F family - select psv page

  //-------------------------------------------------------------------------//
  //    Copy flash table data from "my_constants" to user scratch pad        //
  //    data ram array "my_scratchpad".                                      //
  //  NOTE:    Memcopy function encodes a REPEAT instruction with indirect   //
  //           memory move instruction with auto post increment for both      //
  //           source and destination address.                                //
  //-------------------------------------------------------------------------//

  memcpy(p,(int unsigned *) __builtin_psvoffset(&my_constants),sizeof(my_scratchpad)/sizeof(char));
}
```

4.1.3 MAPPING FLASH INTO PSV

If placing whole constants tables or copying partial Flash data constants tables as needed into RAM is not feasible, the PSV page method can be used to map Flash into the PSV virtual data memory space. This is done to utilize the indirect data memory access suite of instructions. Avoid using the non-PSV table read instructions for accessing Flash data as they are considerably slower.

4.2 C Compiler Optimization Options

Use the MPLAB C Compiler for PIC24 MCUs and dsPIC DSCs (also known as C30) optimization features.

4.2.1 C COMPILER OPTIMIZATION

For user-enabled full-featured C compilers, use the 02 or 03 optimization settings in MPLAB. This will have a significant effect on the general performance for C code execution. Compiler optimization settings have no effect on either precompiled library files or Assembly language files.

4.2.2 OPTIMIZATION LEVEL 02

C compiler optimization level 02, by default, turns on *all* optional optimizations with the exception of:

- Loop unrolling (`-funroll-loops`)
- Function in-lining (`-finline-functions`)
- Strict aliasing optimizations (`-fstrict-aliasing`)

It also turns on:

- Force copy of memory operands (`-fforce-mem`)
- Frame pointer elimination (`-fomit-frame-pointer`)

4.2.3 OPTIMIZATION LEVEL 03

C compiler optimization level 03 turns on all optimizations specified by the 02 default setting, and also the `in-line-functions` option. This boosts application performance even more, but at the cost of increasing the code size footprint.

Note:	For optimized enabled versions of the C compiler, users can mix or incrementally add optimization options to any of the various compiler base default optimization levels by using C command line options. Refer to **3.5.6 "Options for Controlling Optimizations"** in the *"MPLAB® C Compiler for PIC24 MCUs and dsPIC® DSCs User's Guide"* (DS51284) for more information.

4.2.4 COMPILER DATA MODEL OPTION

Use the large data model with the small scalar model compiler option. Using this combination forces arrays and structures into far memory, which is acceptable since indirect addressing is required. However, enabling the small scalar model compiler option forces everything else into near memory. As previously mentioned, using the large data model option forces all variable accesses to use indirect addressing using working register pointers, which may double and sometimes triple both the code size and the speed of the executable in comparison to the dsPIC33F family for reading or writing to a specific data RAM variable. Refer to the *"MPLAB® C Compiler for PIC24 MCUs and dsPIC® DSCs User's Guide"* (DS51284) for more information.

4.3 Coding Guidelines

Maximize continuous non-branching sequential code sequencing and use zero overhead hardware loops, when feasible, in place of software loops.

4.3.1 BUILT-IN C MACROS

Use the built-in C macros when possible and consider a bit complement C construct.

For example, instead of:

```
LATBbits.LATB5 = !LATBbits.LATB5;
```

Use the built-in:

```
__builtin_btg(&LATB,5);
```

The bit complement built-in offers a significant code size and speed performance improvement. This means fewer instructions and no conditional branching that would flush and force a reload of the instruction fetch pipeline unit.

4.3.2 NEAR VERSUS FAR RAM MEMORY

The first 8K of data RAM space is considered "near" memory. Space above that is considered "far" memory. By default, the compiler sets all user data RAM variables and declarations to near memory as it sequentially encounters variables in the code in the order that C file(s) are compiled. However, when near memory space is full, the compiler will generate compiler errors indicating that it cannot allocate variable(s). This requires the user to either manually allocate the remaining variables using the far attribute or select the large data model compile option. The special significance of near versus far to the compiler is that near data memory accesses are encoded in only one instruction using direct addressing, while accesses to data variables in far space require two to three instructions using indirect addressing.

For this reason, users should insure that frequent, or commonly used data variables, are placed in near memory, while seldom, or less frequently used variables, are forced into far memory if near memory is full using the C compiler `far` attribute.

4.3.3 SEQUENTIAL CODE GROUPING

Group as much sequential executable code in the largest contiguous sections possible that are undisturbed by any program flow instructions such as branches, calls, `goto`, etc. Defer or group C flow control statements such as `if`, `else`, `for`, and `while`, as much as possible in relation to straight-line code. This will insure the instruction pipeline is efficient and is disturbed as little as possible so it is not flushed and stalled while reloading. Program flow instructions always flush the instruction pipeline and add additional instruction cycles.

4.3.4 OPTIMIZING CPU INTERRUPTS

Minimize the frequency of peripheral CPU interrupts for those peripherals with data buffers. Peripherals with four to eight byte/word receive or transmit FIFO buffers allow the user to select interrupts based on the amount of data in the FIFO. Whenever possible, set the interrupt based on when the FIFO is full rather than on the first byte/word. This will minimize the number of interrupts and the overhead associated with interrupt latency and suspension of the interrupted code. Interrupt latency for the dsPIC33E/PIC24E family of devices is nine to 13 instruction cycles, and five instruction cycles for the dsPIC33F/PIC24H family of devices. Due to their higher MIPS rating, the instruction cycle time for dsPIC33E/PIC24E devices is much less than that of dsPIC33F/PIC24H devices.

Note:	The dsPIC33E/PIC24E family of devices can have either 13 fixed or nine to 13 variable latency (i.e., user-selectable) instruction cycles.

4.3.5 ISR C FUNCTION CALL LIMITATIONS

Do not call C functions from within an Interrupt Service Routine (ISR). Since the compiler can make no assumptions about registers that may be effected by a subroutine called from within a hardware triggered event, it causes the compiler to save all the working registers (plus a few others) on the stack. This adds considerably more overhead and latency to the ISRs. If absolutely necessary, consider copying the subroutine code directly into the ISR.

4.4 Application Resource Configuration

4.4.1 DMA CONSIDERATIONS

New features in the dsPIC33F/PIC24H families allow the DMA memory buffers to be assigned anywhere in available data memory. Certain devices implement dual-port RAM and some do not (refer to the **"Memory Organization"** chapter of the specific device data sheet for availability).

If the user does not assign the DMA buffers into the dual-port RAM region, either by choice or because it's not available on the target device, the memory bus arbiter must arbitrate simultaneous bus master access requests to the same shared single ported memory resource.

Depending on the device, there are up to four data memory bus masters consisting of the CPU, DMA, USB, and the ICD debugger. The bus arbiter, based on the user-selected priority scheme, will prioritize and interleave bus master requests on an instruction cycle-by-cycle basis for data memory accesses. Lower priority bus master requests will be stalled until all active or pending higher priority requests are serviced. The user should therefore consider these factors when choosing the application data memory resource configuration. The MSTRPR register controls the data memory bus master arbitration priority.

Note: Because the data memory arbitration occurs on a instruction cycle-by-cycle basis it is unlikely that peripherals, with a much slower input/output data rate compared to the CPU, even with several DMA channels active, would have a significant effect on CPU data memory performance. However, the higher the cumulative sum of the data bandwidth from all DMA enabled peripherals combined, increases the probability that a lower priority bus master will become stalled at some point. Combined with devices that incorporate a USB bus master that is active as well and the probability increases again.

For these reasons, on devices with dual-port RAM, the user should always define DMA buffers in the dual-port RAM region if available. There is no arbitration required for the DMA to the dual port data RAM region and therefore no DMA arbitration relative to other bus masters. This alleviates any possibility of DMA access stalls to the dual port data memory region, regardless of the priority of any other bus master such as the CPU, USB or ICD debugger.

The following five code examples show how DMA buffers can be allocated.

EXAMPLE 4-2:

```
//------------------------------------------------------------------------------------------
//Example 1: Assign a 32-bit pointer and allocate a 32 word buffer in dual port
//data ram in Extended Data Memory space. This is a compiler managed buffer.
//------------------------------------------------------------------------------------------
   __eds__ unsigned int BufferA[32] __attribute__((eds,space(dma)));
```

EXAMPLE 4-3:

```
//------------------------------------------------------------------------------------------
//Example 2:  Assign a 16-bit pointer and allocate a 32 word buffer in dual port
//data ram in Extended Data Memory space. This is a compiler managed buffer.
//------------------------------------------------------------------------------------------
   unsigned int BufferA[32] __attribute__((eds,space(dma)));
```

EXAMPLE 4-4:

```
//------------------------------------------------------------------------------------------
//Example 3:  Assign a 32-bit pointer and allocate a 32 word buffer somewhere
//in data ram in Extended Data Memory space as determined by the compiler.
//This is a compiler managed buffer.
//------------------------------------------------------------------------------------------
   __eds__ unsigned int BufferA[32] __attribute__((eds));
```

EXAMPLE 4-5:

```
//-------------------------------------------------------------------------------------------
//Example 4: Assign a 16-bit pointer and allocate a 32 word buffer at address
//0x1000 in data ram space. This is NOT a compiler managed buffer.
//-------------------------------------------------------------------------------------------
   unsigned int BufferA[32] __attribute__(space(data),address(0x1000));
```

EXAMPLE 4-6:

```
//-------------------------------------------------------------------------------------------
//Example 5: Assign a 32-bit pointer and allocate a 32 word buffer at address
//0x84000 in extended data space. This is NOT a compiler managed buffer.
//-------------------------------------------------------------------------------------------
   __eds__ unsigned int BufferA[32] __attribute__(space(eds),address(0x8400));
```

APPENDIX A: REVISION HISTORY

Revision A (July 2010)

This is the initial released version of this document.

Revision B (April 2011)

This revision includes the following updates:

- Updated **"Introduction"**
- Updated the following in **"Operating Range"**:
  - Changed the operating range to 3.0V to 3.6V
  - Updated VDDCORE to VCAP
- Updated **"Package Migration Considerations"**
- Added the following in the Registers section in **"CPU Architecture and Instruction Set"**: The DOSTARTH and DOSTARTL registers are read-only in the dsPIC33E/PIC24E devices.
- Updated the following in the Memory Size and Organization section in **"Data Memory"**:
  - Updated the second paragraph
  - Added a note
- Updated the second paragraph in the Memory Size and Organization section in **"Flash Program Memory"**
- Updated the note in the Pinouts section in **"I/O Ports"**
- Updated the first paragraph in the Registers section in **"Reset"**
- Updated the following in the Feature Enhancements section, in **"Output Compare"**: "Optional tri-stating of Fault pin on a Fault event" is updated to "Optional tri-stating of PWM output on a Fault event"
- Added two features in the list of additional enhancements and new features in **"High-Speed PWM"**
- Updated the third paragraph in the Registers section in **"CodeGuard™ Security"**
- Updated the title and removed all of the notes in **"Additional Device Differences"**
- All references to Flash memory and program Flash memory have been changed to Flash program memory
- All references to auxiliary Flash memory have been changed to auxiliary Flash program memory
- Other minor changes to the text and formatting updates were incorporated throughout the document

Revision C (July 2011)

This revision includes the following updates:

- Changed the title of the document to include performance enhancement
- Removed the CLKDIV and PLLDIV SFRs from **TABLE 2-2: "SFR Differences for dsPIC33E/PIC24E Oscillator"**
- Removed the primary PLL VCO input range from **Section 2.9.2 "Electrical Characteristics"**
- Removed the default state of the DOZE bits in **Section 2.10.1 "Registers"**
- Updated the ADxCON2 SFR difference description in **TABLE 2-5: "SFR Changes for dsPIC33E/PIC24E ADC Module"**
- Updated the Note box in **Section 2.20 "Serial Peripheral Interface (SPI)"**
- Add a note regarding availability of the Motor Control PWM in **Section 2.15 "High-Speed PWM"**
- Added **3.0 "Additional Device Differences"**
- Added **4.0 "Performance Enhancement Techniques"**, which replaces "General Guidelines for Optimal Software Performance in dsPIC33E/PIC24E"
- Replaced all references to the *"dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814 Data Sheet"* (DS70616) with general data sheet references
- Minor changes to text and updates to formatting have been incorporated throughout the document

Revision D (December 2011)

This revision includes the following updates:

- Updated the maximum operating frequency to 70 MIPS
- Updated the maximum system clock frequency (Fosc) to 140 MHz
- Updated the High-Speed PWM module resolution for duty cycle, phase shift, dead time and period to 7.14 ns (@ 70 MIPS)
- Updated the LPRC Oscillator feature for dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, AND PIC24EPXXXGP/MC20X devices in the Device Differences table (see Table 3-1)

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Fax: 66-2-694-1350

EUROPE

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Fax: 43-7242-2244-393

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Tel: 45-4450-2828
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Fax: 34-91-708-08-91

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Fax: 44-118-921-5820

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